JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
DEPARTMENT OF ECE

M.Tech. VLSI SYSTEM DESIGN 2005/06

COURSE STRUCTURE

Course No.	Subject	Contact Hrs. / wk.	Credits
FIRST SEMESTER			
	VLSI Technology & Design	4	8
	Digital System Design	4	8
	Analog IC Design	4	8
	Electronic Design Automation Tools	4	8
Elective –I		4	8
	Computational Techniques in Micro Electronics		
	Digital Data Communications		
	CPLD and FPGA Architecture and Applications		
Elective –II		4	8
	VHDL Modeling of Digital Systems		
	Modelling and Synthesis with Verilog HDL		
	Embedded Systems Concepts		
	HDL Programming & EDATools Laboratory	3	4
SECOND SEMESTER			
	Algorithms for VLSI Design Automation	4	8
	Design for Testability	4	8
	Low Power VLSI Design	4	8
	Scripting Language for VLSI Design Automation	4	8
Elective-III		4	8
	Hardware Software Co-Design		
	System Modeling & Simulation		
	Network Security and Cryptography		
Elective-IV		4	8
	DSP Processors and Architectures		
	Advanced Operating Systems		
	Advanced Computer Architecture		
	Mixed Signal Laboratory	3	4
THIRD & FOURTH SEMESTERS			
	SEMINAR		8
	PROJECT		24
	TOTAL CREDITS		136

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DEPARTMENT OF ECE

M.Tech.(VLSI) – I Semester **2005/06**

VLSI TECHNOLOGY & DESIGN

UNIT – I:
REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi CMOS) Technology trends and projections.

UNIT – II:
BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids-Vds relationships, Threshold voltage V_t, G_m, G_{ds} and W_o, Pass Transistor, MOS,CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model,Latch-up in CMOS circuits.

UNIT – III:
LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias , Scalable Design rules ,Layout Design tools.

UNIT – IV:
LOGIC GATES & LAYOUTS: Static complementary gates, switch logic, Alternative gate circuits , low power gates, Resistive and Inductive interconnect delays.

UNIT – V:
COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks, Gate and Network testing.

UNIT – VI:
SEQUENTIAL SYSTEMS: Memory cells and Arrays, clocking disciplines, Design ,power optimization, Design validation and testing.

UNIT – VII:
FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

UNIT – VIII:
INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and printing; Hardware/Software Co-design, chip design methodologies- A simple Design example-

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et . al(3 authors) PHI of India Ltd.,2005
2. Modern VLSI Design, 3rd Edition, Wayne Wolf ,Pearson Education, fifth Indian Reprint,2005.

REFERENCES:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.

CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.

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DEPARTMENT OF ECE
M.Tech.(VLSI) – I Semester **2005/06**

DIGITAL SYSTEM DESIGN

UNIT – I:
DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

UNIT – II:
SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT – III:
FAULT MODELING: Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.
TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT – IV:
TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT – V:
FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT – VI:
PROGRAMMING LOGIC ARRAYS: Design using PLA's, PLA minimization and PLA folding.

UNIT – VII:
PLA TESTING: Fault models, Test generation and Testable PLA design.

UNIT – VIII:
ASYNCHRONOUS SEQUENTIAL MACHINE: fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXT BOOKS:

1. Z. Kohavi – "Switching & finite Automata Theory" (TMH)
2. N. N. Biswas – "Logic Design Theory" (PHI)
3. Nolman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

REFRENCE BOOKS:

1. M. Abramovici, M. A. Breues, A. D. Friedman – “Digital System Testing and Testable Design”, Jaico Publications
2. Charles H. Roth Jr. – “Fundamentals of Logic Design”.
3. Frederick. J. Hill & Peterson – “Computer Aided Logic Design” – Wiley 4th Edition.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
DEPARTMENT OF ECE
M.Tech.(VLSI) – I Semester 2005/06

ANALOG IC DESIGN

UNIT I
INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR:
Advanced MOS Modelling ,Large Signal And Small Signal Mo0delling For BJT/Basic Current Mirrors And Single Stage Ampliers:Simple CMOS Current Mirror, Common Source ,Common Gate Amplifier With Current Mirror Active Load . Source Follower With Current Mirror To Supply Bias Current , High Output Impedence Current Mirrors And Bipolar Gain Stages. Frequency Response.

UNIT II
OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION:
Two Stage CMOS Operational Amplifier. Feedback And Operational Amplifier Compensation.Advanced Current Mirror.Folded –Cascode Operational Amplifier, Current Mirror Operational Amplifier.Fully Differential Operational Amplifier. Common Mode Feedback Circuits. Current Feedback Operational Amplifier.Comparator. Charge Injection Error.Latched Comparator And Bi CMOS Comparators.

UNIT III
SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS:
MOS, CMOS, Bimos Sample And Hold Circuits.Switched Capacitor Circuits:Basic Operation And Analysis.First Order And Biquard Filters. Charge Injection . Switched Capacitor Gain Circuit.Correlated Double Sampling Technics.Other Switched Capacitor Circuits.

UNIT IV
DATA CONVERTERS:
Ideal D/A & A/D Converters.Quantization Noise. Performance Limitations. Nyquist Rate D/A Converters: Decoders Based Converters.Binary Scaled Converters.Hybrid Converters.Nyquist Rate A/D Converters: Integrating ,Successive Approximation,Cyclic Flash Type, Two Step,Interpolating,Folding And Pipelined,A/D Converters.

UNIT V
OVER SAMPLING CONVERTERS AND FILTERS:
Over Sampling With And Without Noise Shaping .Digital Decimation Filter.High Order Modulators.Band Pass Over Sampling Converter. Practical Considerations.Continuous Time Filters.

TEXT BOOKS:

1. 1.D.A.JOHN & KEN MARTIN: Analog Integrated Circuit Design. John Wiley,1997.

REFERENCE

1. GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley , 1986.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
DEPARTMENT OF ECE

M.Tech.(VLSI) – I Semester **2005/06**

ELECTRONIC DESIGN AUTOMATION TOOLS

UNIT I

IMPORTANT CONCEPTS IN VERILOG:

Basics Of Verilg Language, Operators, Hierarchy,Procedures And Asignments,Timing Controls And Delay. Tasks And Functions Control Statements, Logic-Gate Modeling, Modeling Delay, Altering Parameters, Other Verilog Features.

UNIT II

SYNTHESIS AND SIMULATION USING HDLS:

Verilog And Logic Synthesis. VHDL And Logic Synthesis, Memory Synthesis,FSM Synthesis,Memory Synthesis, Performance-Driven Synthesis. Simulation-Types Of Simulation, Logic Systems Working Of Logic Simulation,Cell Models, Delay Models State Timing Analysis,Formal Verification, Switch-Level Simulation Transistor-Level Simulation. CAD Tools For Synthesis And Simulation Modelism And Leonardo Spectrum(Exemplar).

UNIT III

TOOLS FOR CIRCUIT DESIGN AND SIMULATION USING PSPICE:

Pspice Models For Transistors, A/D & D/A Sample And Hold Circuits Etc, And Digital System Building Blocks, Design And Analysis Of Analog And Digital Circuits Using PSPICE.

UNIT IV

AN OVER VIEW OF MIXED SIGNAL VLSI DESIGN:

Fundamentals Of Analog And Digitla Simulation,Mixed Signal Simulator Configurations, Understanding Modeling, Integration To CAE Environmets, Analyses Of Analog Circuits Eg.A/D, D/A Converters, Up And Down Converters, Companders Etc.

UNIT V

TOOLS FOR PCB DESIGN AND LAYOUT:

An Overview Of High Speed PCB Design, Design Entry, Simulation And Layout Tools For PCB. Introduction To Orcad PCB Design Tools.

TEXTBOOKS

1. J.Bhaskar, A Verilog Primer, BSP, 2003.
2. J.Bhaskar, A Verilog HDL Synthesis BSP, 2003
3. M.H.RASHID:SPICE FOR Circuits And Electronics Using PSPICE (2/E)(1992) Prentice Hall.

REFERENCES

1. ORCAD: Technical Reference Manual ,Orcad, USA.
2. SABER: Technical Reference Manual, Analogy Nic, USA.
3. M.J.S.SMITH :Aplication-Specific Integrated Circuits(1997). Addison Wesley
4. J.Bhaskar, A VHDL Synthesis Primer, BSP, 2003.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
DEPARTMENT OF ECE
M.Tech.(VLSI) – I Semester **2005/06**

COMPUTATIONAL TECHNIQUES IN MICROELECTRONICS
(ELECTIVE I)

Linear And Non-Linear Circuit Simulation Techniques-Algorithms And Computational Methods; Transient Analysis; Frequency Domain Analysis; Moment Methods; Sensitivity Analysis Timing Simulation. Numerical Solution Of Differential Equations-FEM,FVM And FDM, Grid Generation, Error Estimates, Transient And Small Signal Solutions Applications To Device And Process Simulation. Introduction To VHDL Medeling. Layout Algorithms ,Yield Estimation Algorithms. Symbolic Analysis And Synthesis Of Analog Ics.

Introduction To Physical Design, Part Training Algorithms , Algorithms For Placement And Floor Planning ,Global Routing And Detailed Routing.

TEXT BOOKS:

1. Computer Aided Analysis Of Electronics Circuits : Algorithms And Computational Techniques. L.O.CHUA AND P.M.LIN, Prentice –Hall 1975.
2. Electronics Circuits And Simulation Methods, L.PALLAGE,R.ROHRER AND C.VISWESWARAIAH, Mc. Graw Hall,1995.
3. Algorithms For VLSI Physical Design Automation, NAVEED SHEWANI, Kluwer Academic ,1993.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
DEPARTMENT OF ECE
M.Tech.(VLSI) – I Semester **2005/06**

DIGITAL DATA COMMUNICATIONS
(ELECTIVE I)

UNIT I
DIGITAL MODULATION TECHNIQUES
FSK , MSK , BPSK , QPSK , 8-PSK , 16-PSK , 8- QAM , 16- QAM , Band width efficiency carrier recovery , DPSK , clock recovery , Probability of error and bit error rate.

UNIT II
Data Communications ; Serial , Parallel configuration , Topology , Transmission modes , codes , Error Control Synchronization, LCU.

UNIT III
Serial and Parallel Interfaces , Telephone Networks and Circuits , Data modems

UNIT IV
Data Communication Protocols , Character and block Mode ,Asynchronous and Synchronous Protocols, public Data Networks , ISDN.

UNIT V
LOCAL AREA NETWORKS : token ring , Ethernet , Traditional , Fast and GIGA bit Ethernet, FDDI

UNIT VI
DIGITAL MULTIPLEXING : TDM , T1 carrier , CCITT , CODECS, COMBO CHIPS , North American Hierarchy , Line Encoding , T-carrier , Frame Synchronization Inter Leaving Statistical TDM FDM , Hierarchy ,Wave Division Multiplexing .

UNIT VII
WIRELESS LANS
IEEE 802.11 Architecture Layers , Addressing, Blue Tooth Architecture Layers, l2 Cap , Other Upper Layers .

UNIT VIII
MULTI MEDIA
Digitalizing Video and Audio Compression Streaming Stored and Live Video and Audio , Real Time Interactive Video and Audio , VOIP

TEXT BOOKS

1. Electronic communication systems , fundamentals through advanced - W. TOMASI ,Pearson 4th Edition .
2. Data communication and networking - B.A. Forouzen

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DEPARTMENT OF ECE

M.Tech.(VLSI) – I Semester **2005/06**

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS (ELECTIVE I)

UNIT I

Programmable logic : ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD's – CPLD (Mach 1 to 5); Cypres FLASH 370 Device Technology, Lattice pLSI's Architectures – 3000 Series – Speed Performance and in system programmability.

UNIT II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping jfor FPGAs, Case studies – Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and their speed performance.

UNIT III

Finite State Machines (FSM): Top Down Design – State Transition Table, state assignments for FPGAs. Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL. Alternative realization for state machine chart suing microprogramming. Linked state machines. One – Hot state machine, Petrinetes for state machines – basic concepts, properties. Extended petrinetes for parallel controllers.

Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT IV

FSM Architectures and Systems Level Design: Architectures centered around non-registered PLDs. State machine designs centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. K Application of One – Hot method. System level design – controller, data path and functional partition.

UNIT V

Digital Front End Digital Design Tools for FPOGAs & ASICs: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of paraller adder cell, paraller adder sequential circuits, counters, multiplexers, parallel controllers.

SUGGESTED BOOKS:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, jPrentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publicatgions, 1994.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
DEPARTMENT OF ECE

M.Tech.(VLSI) – I Semester **2005/06**

VHDL MODELLING OF DIGITAL SYSTEMS
(ELECTIVE II)

UNIT I
INTRODUCTION :

An Overview Of Design Procedures Used For System Design Using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place And Route. Design Verification Tools. Examples Using Commercial PC Based On VHDL Elements Of VHDL Top Down Design With VHDL Subprograms. Controller Description VHDL Operators.

UNIT II
BASIC CONCEPT IN VHDL:

Characterizing Hardware Languages, Objects And Classes, Signal Assignments, Concurrent And Sequential Assignments. Structural Specification Of Hardware: Parts Library Wiring Of Primitives, Wiring Interactive Networks, Modeling A Test Bench Binding Alternative Top Down Wiring.

UNIT III
DESIGN ORGANIZATIN AND PARAMETERIZATION:

Definition And Usage If Subprograms, Packaging Parts And Utilities, Design Parametrization, Design Configuration, Design Libraries, Utilities For High –Level Descriptions-Type Declaration And Usage, VHDL Operators, Subprogram Parameter Types And Overloading, Other Types And Type Related Issues, Predefined Attributes, User Defined Attributes, Packing Basic Utilities.

UNIT IV
DATA FLOW DESCRIPTION IN VHDL

Multiplexing And Data Selection, State Machine Description, Open Collector Gates, Three State Bussing A General Data Flow Circuit, Updating Basic Utilities. Behavioral Description Of Hardware: Process Statement Assection Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design.

UNIT V
CPU MODELLING FOR DESCRIPTION IN VHDL:

Parwan CPU, Behavioural Description Of Parawan, Bussing Structure, Data Flow Description Test Bench For The Parwan CPU. A More Realistic Parwan. Interface Design And Modeling. VHDL As A Modelling Language.

TEXT BOOKS:

1. Z.NAWABI : VHDL Analysis And Modelling Of Digital Systems. (2/E), Mcgraw Hill, (1998)

<u>REFERENCE:</u>

1. PERRY : VHDL, (3/E) Mcgraw Hill

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
DEPARTMENT OF ECE

M.Tech.(VLSI) – I Semester **2005/06**

MODELING AND SYNTHESIS WITH VERILOG HDL
(ELECTIVE II)

UNIT I
HARDWARE MODELING WITH THE VERILOG HDL :
Hardware Encapsulation – The Verilog Module, Hardware Modeling Verilog Primitives, Descriptive Styles, Structural Connections, Behaviral Description In Verilog, Hierarchical Descriptions Of Hardware, Structured (Top Down) Design Methodology, Arrays Of Instances, Using Verilog For Synthesis, Language Conventions, Representation Of Numbers.

UNIT II
LOGIC SYSTEM, DATA TYPES AND OPERATORS FOR MODELING IN VERILOG HDL :
User-Defined Primitives, User Defined Primitives – Combinational Behavior User-Defined Primitives – Sequential Behavior, Initialization Of Sequential Primitives. Verilog Variables, Logic Value Set, Data Types, Strings. Constants, Operators, Expressions And Operands, Operator Precedence Models Of Propagation Delay; Built-In Constructs For Delay, Signal Transitions, Verilog Models For Gate Propagation Delay (Interila Delay), Time Scales For Simulation, Verilog Models For Net Delay (Transport Delay), Module Paths And Delays, Path Delays And Simulation, Inertial Delay Effects And Pulse Rejection.

UNIT III
BEHAVIORAL DESCRIPTIONS IN VERILOG HDL :

Verilog Behaviors, Behavioral Statements, Procedural Assignment, Procedural Continuous Assignments, Procedural Timing Controls And Synchronization, Intra-Assignment, Delay-Blocked Assignments, Non-Blocking Assignment, Intra-Assignment Delay: Non-Blocking Assignment, Simulation Of Simultaneous Procedural Assignments, Repeated Intra Assignment Delay, Indeterminate Assignments And Ambiguity, Constructs For Activity Flow Control, Tasks And Functions, Summary Of Delay Constructs In Verilog, System Tasks For Timing Checks, Variable Scope Revisited, Module Contents, Behavioral Models Of Finite State Machines.

UNIT IV
SYNTHESIS OF COMBINATIONAL LOGIC :

HDL-Based Synthesis, Technology-Independent Design, Benefits Of Synthesis, Synthesis Methodology, Vendor Support, Styles For Synthesis Of Combinational Logic, Technology Mapping And Shared Resources, Three State Buffers, Three State Outputs And Don't Cares, Synthesis Of Sequential Logic Synthesis Of Sequential Udps, Synthesis Of Latches, Synthesis Of Edge-Triggered Flip Flops, Registered Combinational Logic, Shift Registers And Counters, Synthesis Of Finite State Machines, Resets, Synthesis Of Gated Clocks, Design Partitions And Hierarchical Structures.

UNIT V

SYNTHESIS OF LANGUAGE CONSTRUCTS :

Synthesis Of Nets, Synthesis Of Register Variables, Restrictions On Synthesis Of "X" And "Z", Synthesis Of Expressions And Operators, Synthesis Of Assignments, 6 Synthesis Of Case And Conditional Statement, Synthesis Of Resets, Timings Controls In Synthesis, Synthesis Of Multi-Cycle Operations, Synthesis Of Loops, Synthesis If Fork Join Blocks, Synthesis Of The Disable Statement Synthesis Of User-Defined Tasks, Synthesis Of User-Defined Functions, Synthesis Of Specify Blocks, Synthesis Of Compiler Directives. Switch-Level Models In Verilog MOS Transistor Technology, Switch Level Models Of MOS Transistors, Switch Level Models Of Static CMOS Circuits, Alternative Loads And Pull Gates, CMOS Transmission Gates. Bio-Directional Gates (Switches), Signal Strengths, Ambiguous Signals, Strength Reduction By Primitives, Combination And Resolution Of Signal Strengths, Signal Strengths And Wired Logic. Design Examples In Verilog.

TEXTBOOK

1. M.D.CILETTI: Modeling, Synthesis And Rapid Prototyping With The Verilog HDL (1999), Prentice-Hall.

REFERENCE

1. M.G.ARNOLD : Verilog Digital – Computer Design. (1999), Prentice-Hall (PTR).

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
DEPARTMENT OF ECE

M.Tech.(VLSI) – I Semester **2005/06**

HDL PROGRAMMING AND EDA TOOLS LABORATORY

1. Digital Circuits Description using Verilog and VHDL

2. Verification of the Functionality of Designed circuits using function Simulator.

3. Timing simulation for critical path time calculation.

4. Synthesis of Digital circuits

5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.

6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

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DEPARTMENT OF ECE

M.Tech.(VLSI) – I Semester **2005/06**

EMBEDDED SYSTEMS CONCEPTS
(ELECTIVE II)

UNIT I: AN INTRODUCTION TO EMBEDDED SYSTEMS
An Embedded system, processor in the system, other hardware units, software embedded into a system, exemplary embedded systems, embedded system – on – chip (SOC) and in VLSI circuit. Processor and memory organization – Structural Units in a Processor, Processor selection for an embedded system, memory devices, memory selection for an embedded systems, allocation of memory to program cache and memory management links, segments and blocks and memory map of a system, DMA, interfacing processors, memories and Input Output Devices.

UNIT II: DEVICES AND BUSES FOR DEVICE NETWORKS
I/O devices, timer and counting devices, serial communication using the "I2 C" CAN, profibus foundation field bus. and advanced I/O buses between the network multiple devices, host systems or computer parallel communication between the networked I/O multiple devices using the ISA, PCI, PCI-X and advanced buses.

UNIT III: DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM
Device drivers, parallel port and serial port device drivers in a system, device drivers for internal programmable timing devices, interrupt servicing mechanism

UNIT IV: PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C, C++, VC++ AND JAVA
Interprocess communication and synchronization of processes, task and threads, multiple processes in an application, problem of sharing data by multiple tasks and routines, interprocess communication.

UNIT V: HARDWARE – software co-design in an embedded system, embedded system project management, embedded system design and co-design issues in system development process, design cycle in the development phase for an embedded system, use of target systems, use of software tools for development of an embedded system, use of scopes and logic analysis for system, hardware tests. Issues in embedded system design.

TEXT BOOK:

1. Embedded systems: Architecture, programming and design by Rajkamal, TMH

REFERENCE:

1. Embedded system design by Arnold S Burger, CMP
2. An embedded software primer by David Simon, PEA
3. Embedded systems design:Real world design be Steve Heath; Butterworth Heinenann, Newton mass USA 2002
4. Data communication by Hayt.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
DEPARTMENT OF ECE
M.Tech.(VLSI) – II Semester **2005/06**

ALGORITHMS FOR VLSI DESIGN AUTOMATION

UNIT I
PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithimic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III
Layout Compaction, Placement, Floorplanning And Routing Problems, Concepts and Algorithms.

UNIT IV
MODELLING AND SIMULATION: Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT V
LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

UNIT VI
HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aqspects of Assignment problem, High-level Transformations.

UNIT VII
PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT VIII
PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM phsical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Algorithms for VLSI Physical Design Automation ,3rd edition, Naveed Sherwani, Springer International Edition, 2005.

REFERENCES

1. Comoputer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993.
2. Modern VLSI Design:Systems on silicon – Wayne Wolf, Pearson Education Asia, 2nd Edition, 1998

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M.Tech.(VLSI) – II Semester **2005/06**

DESIGN FOR TESTABILITY

UNIT I

Introduction to Test and Design for Testability (DFT) Fundamentals.

Modeling: Modeling digital circuits at logic level, register level and structural models. Levels of modeling.

Logic Simulation: Types of simulation, Delay models, Element evaluation, Hazard detection, Gate level event driven simulation.

UNIT II

Fault Modeling – Logic fault models, Fault detection and redundancy, Fault equivalence and fault location. Single stuck and multiple stuck – Fault models. Fault simulation applications, General techniques for Combinational circuits.

UNIT III

Testing for single stuck faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT IV

Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scans standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT V

Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST): Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.

Introduction to automatic in circuit testing (ICT), JTAG Testing features.

SUGGESTING READING

1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
2. Alfred Crouch, Design for Test for Digital ICs & Embedded Core Systems, Prentice Hall.
3. Robert J.Feugate, Jr., Steven M.Mentyn, Introduction to VLSI Testing, Prentice Hall, Englehood Cliffs, 1998.

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DEPARTMENT OF ECE

M.Tech.(VLSI) – II Semester **2005/06**

LOW POWER VLSI DESIGN

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

MOS/BiCMOS PROCESSES : Bi CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT III

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes ,SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT IV

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models.

UNIT V

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid- mode environment.

UNIT VI

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates. Performance evaluation

UNIT VII

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced BiCMOS Digital circuits. ESD-free Bi CMOS , Digital circuit operation and comparative Evaluation.

UNIT VIII

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOKS

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002

REFERENCES

1. Digital Integrated circuits , J.Rabaey PH. N.J 1996
2. CMOS Digital ICs sung-moKang and yusuf leblebici 3rd edition TMH 2003 (chapter 11)
3. VLSI DSP systems , Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

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SCRIPTING LANGUAGE FOR VLSI DESIGN AUTOMATION

UNIT I
Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.

UNIT II
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables.

UNIT III
Inter process Communication Threads, Compilation & Line Interfacing.

UNIT IV
Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL .

UNIT V
Other Languages: Broad Details of CGI, VB Script, Java Script with Programming Examples.

SUGGESTED READING:

1. Randal L, Schwartz Tom Phoenix, “Learning PERL”, Oreilly Publications, 3rd Edn., 2000
2. Larry Wall, Tom Christiansen, John Orwant, “Programming PERL”, Oreilly Publications, 3rd Edn., 2000.
3. Tom Christiansen, Nathan Torkington, PERL Cookbook, Oreilly Publications, 3rd Edn,2000.

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HARDWARE - SOFTWARE CO-DESIGN
(ELECTIVE III)

UNIT I
CO – DESIGN ISSUES AND CO- SYNTHESIS ALGORITHMS :
Co – Design Models, Architectures, Languages, A Generic Co-Design Methodology, Hardware – Software Synthesis Algorithms : Hardware – Software Partitioning, Distributed System Co-Synthesis.

UNIT II
PROTOTYPING AND EMULATION AND TARGET ARCHITECTURES :
Prototyping and Emulation techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Architecture Specialization Techniques, System Communication infrastructure, Target Architectures and Application System Classes, Architectures for Control Dominated System and Data – Dominated Systems.

UNIT III
COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES :
Modern Embedded Architectures, Embedded Software Development needs, Compilation Technologies, Practical Consideration in a compiler Development Environment.

UNIT IV
DESIGN SPECIFICATION AND VERIFICATION :
Design, Co- Design, The Co- Design Computational Model, Concurrency, coordinating Concurrent Computations, interfacing components, Design Verification, Implementation Verification, Verification Tools, Interface Verification

UNIT V
LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN :
System – Level Specification, Design representation for system level synthesis, System level specification Languages, Heterogeneous Specifications and Multi Language Co – Simulation. The cosyma system and Lycos system.

TEXT BOOKS :

1. Hardware / Software Co – Design Principles and Practice, Kluwer Academic publishers

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SYSTEM MODELLING & SIMULATION
(ELECTIVE III)

UNIT I
Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT II
SIMULATION SOFTWARE
Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT III
BUILDING SIMULATION MODELS
Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT IV
MODELING TIME DRIVEN SYSTEMS
Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

UNIT V
EXOGENOUS SIGNALS AND EVENTS
Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation.

UNIT VI
MARKOV PROCESS
Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

UNIT VII
EVENT DRIVEN MODELS
Simulation diagrams, Queing theory, simulating queing systems, Types of Queues, Multiple servers.

UNIT VIII
SYSTEM OPTIMIZATION
System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation methodogy.

TEXT BOOKS:

1. System Modeling & Simulation, An Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modelling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCE BOOKS

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

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NETWORK SECURITY AND CRYPTOGRAPHY (ELECTIVE III)

UNIT I

INTRODUCTION: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security.
CLASSICAL TECHNIQUES: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT II

MODERN TECHNIQUES: Symplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
ALGORITHMS: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

UNIT II

CONVENTIONAL ENCRYPTION: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.
PUBLIC KEY CRYPTOGRAPHY: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptograpy.

UNIT IV

NUMBER THEORY: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.
MESSAGE AUTHENTICATION AND HASH FUNCTIONS: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT V

HASH AND MAC ALGORITHMS: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.
DIGITAL SIGNATURES AND AUTHENTICATION PROTOCOLS: Digital signatures, Authentication Protocols, Digital signature standards.

UNIT VI

AUTHENTICATION APPLICATIONS: Kerberos, X.509 directory Authentication service.
ELECTRONIC MAIL SECURITY: Pretty Good Privacy, S/MIME.

UNIT VII

IP SECURITY: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.
WEB SECURITY: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.

UNIT VIII

INTRUDERS, VIRUSES AND WORMS: Intruders, Viruses and Related threats.
FIRE WALLS: Fire wall Design Principles, Trusted systems.

TEXT BOOKS

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education., 2000.

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DSP PROCESSORS AND ARCHITECTURES
(ELECTIVE IV)

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV

EXECUTION CONTROL AND PIPELINING

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT V

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT VI

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT VII

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

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ADVANCED OPERTAING SYSTEMS
(ELECTIVE IV)

UNIT I

Introduction to Operating Systems, Type of operating systems.

UNIT II
UNIX –I

Overview of UNIX system, Structure, file systems, type of file, ordinary & Special files, file permissions, Introduction to shell.

UNIT III
UNIX – II

UNIX basic commands & command arguments, Standard input / output Input / output redirection, filters and editors.

UNIT IV
UNIX SYSTEMS CALLS

System calls related file structures, input / output process creation & termination.

UNIT V
INTERPROCESS COMMUNICATION IN UNIX

Introduction, file and record locking, Client – Server example, pipes, FIFOs, Streams & Messages, Name Speces, Systems V IPC,Message queues,Semaphores, Shared Memory, Sockets & TLI.

UNIT VI
INTRODUCTION TO NETWORKS AND NETWORK PROGRAMMING IN UNIX :

Network Primer, TCP/IP – Internet Protocols, Socket Programming – Introduction & overview, UNIX domain protocols, Socket Addresses, Elementary Socket system calls, Simple examples.

UNIT VII
LINUX

Introduction to LINUX System, editors and utilities, type of shells.

UNIT VIII
LINUX OPERATIONS

Shell operations, file structure, file management, Operations.

TEXT BOOKS

1. The design of the UNIX Operating Systems – Maurice J.Bach (PHI)
2. The UNIX Programming Environment (PHI) – Kernighan & Pike.
3. UNIX Network Programming - W.Richard Stevens (PHI) – 1998.
4. The Complete reference LINUX – Richard Peterson (TMH)
5. UNIX User Guide – Ritchie & Yates.

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ADVANCED COMPUTER ARCHITECTURE
(ELECTIVE IV)

UNIT I
Fundamentals of Computer design- Technology trends- cost- measuring and reporting performance quantitative principles of computer design.

UNIT II
Instruction set principles and examples- classifying instruction set- memory addressing- type and size of operands- addressing modes for signal processing-operations in the instruction set- instructions for control flow- encoding an instruction set.-the role of compiler

UNIT III
Instruction level parallelism (ILP)- over coming data hazards- reducing branch costs – high performance instruction delivery- hardware based speculation- limitation of ILP

UNIT IV
ILP software approach- compiler techniques- static branch protection- VLIW approach- H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT V
Memory hierarchy design- cache performance- reducing cache misses penalty and miss rate – virtual memory- protection and examples of VM.

UNIT VI
Multiprocessors and thread level parallelism- symmetric shared memory architectures- distributed shared memory- Synchronization- multi threading.

UNIT VII
Storage systems- Types – Buses - RAID- errors and failures- bench marking a storage device- designing a I/O system.

UNIT VIII
Inter connection networks and clusters- interconnection network media – practical issues in interconnecting networks- examples – clusters- designing a cluster

TEXT BOOKS
1. Computer Architecture A quantitative approach 3rd edition John L. Hennessy & David A. Patterson Morgan Kufmann (An Imprint of Elsevier)

REFERENCES
1. Computer Architecture and parallel Processing - Kai Hwang and A.Briggs International Edition McGraw-Hill.
2. Advanced Computer Architectures, Dezso Sima, Terence Fountain, Peter Kacsuk, Pearson.

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MIXED SIGNAL LABORATORY

1. Analog Circuits Simulation using Spice
2. Mixed Signal Simulation Using Mixed Signal Simulators.
3. Layout Extraction for Analog & Mixed Signal Circuits.
4. Parasitic Values Estimation from Layout.
5. Layout Vs Schematic
6. Net List Extraction
7. Design Rule Checks