



**Gokaraju Rangaraju Institute of Engineering and Technology**  
**Remedial School**  
**A.Y:2022-23, Remedial Classes Schedule**

<b>SUBJECT</b>	<b>DATES</b>	<b>TIMINGS</b>
PROBABILITY & STATISTICS	12/7,13/7,14/7, 15/7	3:00 PM -4:00PM
DIGITAL LOGIC DESIGN	18/7, 19/7, 20/7, 21/7	3:00 PM -4:00PM

**Dean-Remedial School**

## Attendance

ROLL.NO	18/7/2023	19/7/2023	20/7/2023	21/7/2023
21241A059A	P	P	A	P
21241A05A0	P	A	P	P
21241A05Y3	A	A	P	P
21241A05U3	A	P	P	A
21241A05Y4	P	P	P	P
22248A0509	P	P	A	P
21241A05A7	A	A	P	A
21241A05J9	P	P	P	P
21241A050E	P	A	P	P
21241A05D5	P	P	A	P
21241A05X3	P	P	P	P
21241A05J4	P	P	P	P
21241A05Q0	A	A	A	A
21241A05A9	P	P	P	P
21241A0579	A	A	A	A
21241A0531	P	P	P	P
21241A05D1	P	P	P	P
21241A0569	A	A	A	A
21241A055E	A	A	A	A

21241A05A6	P	P	P	P
21241A05E0	A	P	P	P
21241A05P7	A	P	P	P
21241A05W9	P	P	P	A
21241A05U0	P	P	P	A
21241A05S7	P	A	P	A
22248A0503	P	A	P	A
22248A0510	P	P	P	P
21241A05U2	P	P	P	A
21241A0513	P	P	P	A
21241A051E	P	P	P	P
21241A05F3	A	P	A	P
21241A055E	P	P	P	P
21241A05A6	P	A	P	P
21241A05E0	A	P	A	P
21241A05P7	P	P	A	P
21241A05W9	P	P	A	P
21241A05U0	P	A	A	P
21241A0513	A	A	A	A
21241A051E	A	A	A	P
21241A05F3	P	P	P	P

## **Class Proofs**



## **Faculty Report on Subject**

### **Subject: DIGITAL LOGIC DESIGN**

Day1: Discussed number conversions and logic gates.

Day 2: Conversion of SOP-POS and POS-SOP.

Day 3: Explained design of Combinational Circuits.

Day 4: Explained design of Sequential Circuits and also memory logic.

Also discussed old question papers and clarified doubts.

### **Feedback**

#### **Feedback on Remedial classes**

<b>S.NO</b>	<b>Item</b>	<b>Feedback</b>
1	Material presented	Excellent

2	Doubts clarification	Very Good
3	Coverage of important topics	Excellent
4	Teaching Clarity	Excellent

**Signature of Dean – RS**

### **Report on Remedial classes**

The current remedial classes have been conducted for current second year B.Tech students. The students are given extra coaching in current second year subjects to prevent failure rate. The basis for student list is the students having backlogs in their I year and current LE students.

The following is the transition rate:

	Name of the	Number	Number	Transition
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	Subject	of students enrolled	of Students Passed	Rate
1	DIGITAL LOGIC DESIGN			