ACADEMIC REGULATIONS PROGRAMME STRUCTURE AND DETAILED SYLLABUS

GR22

Master of Technology VLSI

(Effective for the students admitted from the Academic Year 2022-23)

GOKARAJU RANGARAJU
INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Autonomous)

GOKARAJU RANGARAJU

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ACADEMIC REGULATIONS
PROGRAMME STRUCTURE
&
DETAILED SYLLABUS

Master of Technology
VLSI

(Two Year Regular Programme)
(Applicable for Batches Admitted from 2022-23)

GOKARAJU RANGARAJU

INSTITUTE OF ENGINEERING AND TECHNOLOGY

Bachupally, Kukatpally, Hyderabad, Telangana, India- 500090

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
HYDERABAD

Academic Regulations for M.Tech. (Regular) under GR22

(Applicable for Batches Admitted from 2022-23)

Post Graduate Degree Programme in Engineering and Technology (PG)

Gokaraju Rangaraju Institute of Engineering & Technology (GRIET) offers a 2-year (4 Semesters) Master of Technology (M.Tech.) degree programme. The following programmes are offered in GRIET.

S.No	Department	Programme Code	Programme
1	Civil Engineering	20	M.Tech. Structural Engineering
2	Electrical and Electronics Engineering	43	M.Tech. Power Electronics
3	Mechanical Engineering	52	M.Tech. Design for Manufacturing
4	Electronics and Communication Engineering	57	M.Tech. VLSI
5	Computer Science and Engineering	58	M.Tech. Computer Science and Engineering
6	Information Technology	B0	M.Tech. Data Science

GR22 Regulations shall govern the above programmes offered by the Departments with effect from the students admitted to the programmes in 2022-23 academic year is given below

1. **Medium of Instruction:** The medium of instruction (including examinations and reports) is English.
2. **Admission:** Admission into the M.Tech. Programme in any discipline shall be made subject to the eligibility and qualifications prescribed by the University from time to time. Admissions shall be made either on the basis of the merit rank obtained by the student in GATE, PGCET conducted by the APSCHE for M.Tech. Programmes or on the basis of any other order of merit approved by the University, subject to reservations as prescribed by the Government from time to time.
3. **Programme Pattern:**
   a) Each Academic year of study is divided into two semesters.
   b) Minimum number of instruction days in each semester is 90.
   c) The total credits for the Programme are 68.

d) Grade points, based on percentage of marks awarded for each course will form the basis for calculation of SGPA (Semester Grade Point Average) and CGPA (Cumulative Grade Point Average).

e) A student has a choice of registering for credits from the courses offered in the programme.

f) All the registered credits will be considered for the calculation of final CGPA.

g) Each Semester shall have 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)'. Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) are taken as 'references' for the present set of Regulations. The terms 'SUBJECT' and 'COURSE' imply the same meaning here and refer to 'Theory Subject', or 'Lab Course', or 'Design/Drawing Subject', or 'Mini Project with Seminar', or 'Dissertation', as the case may be.

h) Course Classification: All courses offered for all undergraduate programmes in M.Tech. degree programmes are broadly classified as follows.

S. No.	Broad Course Classification	Course Group/ Category	Course Description
1	PC	Professional Core	Includes Core Courses related to the parent discipline/department/ branch of Engineering
2	PE	Professional Elective	Includes Elective Courses related to the parent discipline/ department/ branch of Engineering
3	OE	Open Elective	Elective Courses from other technical and/or emerging subjects
4	Audit	Audit Courses	Mandatory non creditable courses
5	PW	Project Work/Dissertation	Mini Project work, Dissertation Phase-I, II.

4. Award of M.Tech. Degree: A student will be declared eligible for the award of the M.Tech. Degree if he/she fulfills the following academic requirements:

a) A student shall be declared eligible for the award of M.Tech. degree, if he/she pursues the course of study and completes it successfully in not less than two academic years and not more than four academic years.

b) A Student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the date of admission, shall forfeit his/her seat in M.Tech. programme.

c) The Degree of M.Tech. shall be conferred by Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad, on the students who are admitted to the programme and fulfilled all the requirements for the award of the degree.

5. Attendance Requirements

a) A student shall be eligible to appear for the semester end examinations if he/she puts in a minimum of 75% of attendance in each course concerned in the semester.

b) Condonation of shortage of attendance up to 10% (65% and above and below 75%) in a semester may be granted. A committee headed by Dean (Academic Affairs) shall be the deciding authority for granting the condonation.

c) Students who have been granted condonation shall pay a fee as decided by the Academic Council.

d) Students whose attendance is less than 65% in any course are detained and are not eligible to take their end examination of that course. They may seek re-registration for that course when offered next with the academic regulations of the batch into which he/she gets re-registered.

e) A student shall put in a minimum required attendance in at least three theory subjects (excluding audit (non-credit course) in first Year I semester for promotion to first Year II Semester.

f) A student shall put in a minimum required attendance in at least three theory subjects (excluding audit (non-credit course) in first Year II semester for promotion to second Year I Semester.

6. Paper Setting, Evaluation of Answer Scripts, Marks and Assessment

a) Paper setting and Evaluation of the Answer Scripts shall be done as per the procedures laid down by the Academic Council of the College from time to time.

b) The following is the division of marks between internal and external evaluations.

S. No	Components	Internal Evaluation	External Evaluation	Total
1	Theory	40	60	100
2	Practical	40	60	100
3	Mini Project	100	--	100
4	Dissertation	50	50	100

c) Continuous Internal Evaluation and Semester End Examinations: The assessment of the student's performance in each course will be based on Continuous Internal Evaluation (CIE) and Semester-End Examination (SEE). The marks for each of the component of assessment are fixed as shown in the following Table.

Assessment Procedure

S. No	Component of Assessment	Marks Allotted	Type of Assessment	Scheme of Examinations
1	Theory	40	Internal Examination & Continuous Evaluation	1) Two mid semester examination shall be conducted for 30 marks each for a duration of 120 minutes. Average of the two mid exams shall be considered **i) Subjective – 20 marks** **ii) Objective – 10 marks** 2) Continuous Evaluation is by conducting Assignments and Quiz exams at the end of each unit **i) Assignment – 5 marks** **ii) Quiz/Subject Viva-voce/PPT/Poster Presentation/ Case Study on a topic in the concerned subject – 5 marks**
		60	Semester end examination	The semester-end examination is for a duration of 3 hours
2	Practical	40	Internal Examination & Continuous Evaluation	One internal lab examination towards the end of course for a duration of 90 minutes with a viva of 5 minutes. **i) Internal Exam-10 marks** **ii) Viva voce – 10 marks** **iii) Continuous Assessment- 10 marks** **iv) G-Lab on Board(G-LOB) (Case study inter threading of all experiments of lab)/ Laboratory Project/Prototype Presentation/App Development - 10 marks**
		60	Semester end examination	The semester-end examination is for a duration of 3 hours. **i) write-up (algorithm/flowchart/procedure) as per the task/experiment/program - 10 marks** **ii) task/experiment/program-15 marks** **iii) evaluation of results -15 marks** **iv) write-up (algorithm/flowchart/procedure) for another task/experiment/program- 10 marks** **v) viva-voce on concerned laboratory course - 10 marks**

d) Project Review Committee: For approval and evaluating mini project, Dissertation-I and Dissertation-II, a Project Review Committee (PRC) will be constituted by the Head of the Department. The composition of PRC is as follows

i) Head of the Department

ii) One senior faculty relevant to the specialization

iii) Coordinator of the specialization.

e) Mini Project: The Mini Project is to be taken up with relevance to Industry and is evaluated for 100 marks. Student shall carryout the mini project in consultation with the mini project supervisor. The Project Review Committee (PRC) along with supervisor will review the progress of the mini project during the internal evaluation for 50 marks. Mini Project Viva Voce will be evaluated by the PRC for another 50 marks before the semester end examinations. The student must secure a minimum of 50% of marks in i) internal evaluation and ii) mini project viva voce, to be declared successful. If he fails to obtain the minimum marks, he/she must reappear for the same as and when scheduled.

Internal Evaluation: Tentative presentation dates and marks distribution of the mini project.

S.No	Date	Review	Marks
Internal Marks (50)			
1	First week of the semester	Abstract submission*	10
2	Fourth week of the semester	First Review	10
2	Mid of the semester	Second Review	10
3	Last week of the semester	Last Review	20

Following are the guidelines for the abstract submission

The faculty are requested to check the document submitted in the first review and should contain following:

1. Title of the project and Literature review.
2. Schematic/Block diagram which gives the broad idea of the entire project.
3. Timeline or milestone of the project. It should clearly indicate deliverables/outcomes of the project.
4. Components required with approximate cost.
5. References.
6. Plagiarism check is compulsory for mini project report as per the plagiarism policy of GRIET.

External Evaluation: (50 Marks) The mini project report is presented before PRC along with the supervisor.

Guidelines to award 50 marks:

S. No	Date	Review/ PRC report	Marks
External Evaluation Marks (50)			
1	Last week of the semester	Final Presentation and report Submission	10
2	Project report: Project report should be written as per IEEE guidelines.	Verified by PRC	10
3	Project Deliverables • Hardware prototype • Simulation in any authorized software • Submission of research articles in any Scopus Indexed conference /Journal	Verified by PRC	20
4	Results and Discussion	Verified by PRC	10

f) Dissertation (Phase I & Phase II): Every candidate shall be required to submit a dissertation on a topic approved by the Project Review Committee (PRC).

- The candidate must present in **Dissertation Work Review - I**, in consultation with his/her Dissertation Supervisor, the title, objective and plan of action of his/her Dissertation work to the PRC for approval ***within four weeks*** from the commencement of **Second year First Semester**. Only after obtaining the approval of the PRC can the student initiate the Dissertation work.
- If a candidate wishes to change his/her supervisor or topic of the Dissertation, he/she can do so with the approval of the PRC. However, the PRC shall examine whether or not the change of topic/supervisor leads to a major change of his/her initial plans of Dissertation proposal. If yes, his/her date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.
- The candidate shall submit his/her Dissertation progress report in two stages at least with a gap of **three** months between them.
- The work on the Dissertation shall be initiated at the beginning of the II year and the duration of the Dissertation is two semesters. A candidate is permitted to submit Dissertation Thesis only after successful completion of all theory and practical courses with the approval of PRC ***not earlier than 40 weeks*** from the date of approval of the Dissertation work. For the approval of PRC, the candidate shall submit the draft copy of thesis to the Head of the Department and make an oral presentation before the PRC.
- **The Dissertation Work Review - II** in II Year I Semester carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and DRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Dissertation Work. A candidate must secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - II. If he/she fails to obtain the minimum required marks, he has to reappear for Dissertation Work Review - II as and when conducted.

- **The Dissertation Work Review - III** in II Year II Sem. carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progress of the Dissertation Work and decide whether the Dissertation is eligible for final submission. A candidate must secure a minimum of 50% of marks to be declared successful in Dissertation Work Review - III. If he/she fails to obtain the required minimum marks, he/she must reappear for Dissertation Work Review - III as and when conducted. For Dissertation Evaluation (Viva Voce) in II Year II Semester there are external marks of 100 and it is evaluated by the external examiner. The candidate must secure a minimum of 50% marks in Dissertation Evaluation (Viva- Voce) examination.
- Dissertation Work Reviews - II and III shall be conducted in Phase I (Regular) and Phase II (Supplementary). Phase II will be conducted only for unsuccessful students in Phase I. The unsuccessful students in Dissertation Work Review - II (Phase II) shall reappear for it at the time of Dissertation Work Review - III (Phase I). These students shall reappear for Dissertation Work Review- III in the next academic year at the time of Dissertation Work Review - II only after completion of Dissertation Work Review - II, and then Dissertation Work Review - III follows. The unsuccessful students in Dissertation Work Review - III (Phase II) shall reappear for Dissertation Work Review – III in the next academic year only at the time of Dissertation Work Review - II (Phase I).
- A student shall present the progress of the dissertation through Dissertation Reviews II and III with at least a gap of three months between the reviews.
- After approval from the DRC, a soft copy of the thesis should be submitted for ANTI-PLAGIARISM Check from the approved agency with a similarity index not more than 24% and the plagiarism report and be included in the final thesis. If the similarity index has more than the required percentage, the student is advised to modify accordingly and resubmit the soft copy of the thesis after one month. The maximum number of re-submissions of thesis after plagiarism check is limited to ***TWO***. The candidate must register for the Dissertation work and work for two semesters. After three attempts, the admission is liable to be cancelled.
- Three copies of the Dissertation Thesis certified by the supervisor shall be submitted to the Institute, after submission of a research paper related to the Dissertation work in a SCOPUS/Web of Science/UGC approved journal. A copy of the submitted research paper shall be attached to thesis.
- The thesis shall be adjudicated by an external examiner selected by the University. For this, the Principal of the Institute shall submit a panel of **three** examiners from among the list of experts in the relevant specialization as submitted by the supervisor concerned and Head of the Department.
- If the report of the external examiner is unsatisfactory, the candidate shall revise and resubmit the Thesis. If the report of the examiner is unsatisfactory again, the thesis shall be summarily rejected. Subsequent actions for such dissertations may be considered, only on the specific recommendations of the external examiner and /or Dissertation Review Committee. No further correspondence in this matter will be entertained if there is no specific recommendation for resubmission.
- If the report of the examiner is satisfactory, the Head of the Department shall coordinate and decide for the conduct of Dissertation Viva-Voce examination. The Dissertation Viva-Voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who adjudicated the Thesis. The candidate must secure a minimum of 50% of marks in Dissertation Evaluation (Viva-Voce) examination.
- If he/she fails to fulfill the requirements of minimum 50% of marks, he/she will reappear for the Dissertation Viva-Voce examination ***only after three months***. In the reappeared examination also, if he/she fails to fulfill the requirements, he/she will not be eligible for the

award of the degree, unless he/she is asked to revise and resubmit his/her Dissertation Work by the board within a specified time period (within ***four*** years from the date of commencement of his/her first year first semester).

7. **Recounting of Marks in the End Examination Answer Books:** A student can request for re-counting of his/her answer book on payment of a prescribed fee.
8. **Re-evaluation of the End Examination Answer Books:** A student can request for re-evaluation of his/her answer book on payment of a prescribed fee.
9. **Supplementary Examinations:** A student who has failed in an end semester examination can appear for a supplementary examination, as per the schedule announced by the College/Institute.
10. **Malpractices in Examinations:** Disciplinary action shall be taken in case of malpractice during Mid/ End-examinations as per the rules framed by the Academic Council.
11. **Academic Requirements:**

a) A student shall be deemed to have secured the minimum academic requirement in a subject if he / she secures a minimum of 40% of marks (i.e.,16 marks out of 40 marks) in CIE, 40% of marks (i.e.,24 marks out of 60 marks) in SEE and a minimum aggregate of 50%(i.e.,50 marks out of 100 marks) of the total marks in the Semester-end examination (SEE) and Internal Evaluation (CIE) taken together.

The student is eligible to write Semester End Examination of the concerned subject, if the student scores ≥ 40% (16 marks) of 40 Continuous Internal Examination (CIE) marks.

In case, the student appears for Semester End Examination (SEE) of the concerned subject but not scored minimum 40% of CIE marks (16 marks out of 40 internal marks), his performance in that subject in SEE shall stand cancelled inspite of appearing the SEE.

b) A student shall be promoted to the next semester only when he/she satisfies the requirements of all the previous semesters.

c) In order to qualify for the award of M.Tech. Degree, the student shall complete the academic requirements of passing in all the Courses as per the course structure including Seminars and Project if any.

d) In case a student does not secure the minimum academic requirement in any course, he/she has to reappear for the Semester-end Examination in the course, or re-register for the same course when next offered or re-register for any other specified course, as may be required. However, one more additional chance may be provided for each student, for improving the internal marks provided the internal marks secured by a student are less than 50% and he/she failed finally in the course concerned. In the event of taking another chance for re-registration, the internal marks obtained in the previous attempt are nullified. In case of re-registration, the student has to pay the re-registration fee for each course, as specified by the Dean Admissions of College.

e) Grade Points: A 10- point grading system with corresponding letter grades and percentage of marks, as given below, is followed:

Letter Grade	Grade Points	Percentage of marks
O (Outstanding)	10	Marks >= 90
A+ (Excellent)	9	Marks >= 80 and Marks < 90
A (Very Good)	8	Marks >= 70 and Marks < 80
B+ (Good)	7	Marks >= 60 and Marks < 70
B (Above Average)	6	Marks >= 50 and Marks < 60
F (Fail)	0	Marks < 50
Ab (Absent)	0	

Earning of Credit:

A student shall be considered to have completed a course successfully and earned the credits if he/she secures an acceptable letter grade in the range O-B. Letter grade 'F' in any Course implies failure of the student in that course and no credits earned.

Computation of SGPA and CGPA:

The UGC recommends the following procedure to compute the Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

i) $\mathbf{S_k}$ the SGPA of k^{th} semester (1 to 4) is the ratio of sum of the product of the number of credits and grade points to the total credits of all courses registered by a student, i.e.,

$$SGPA\ (S_k) = \sum_{i=1}^{n} (C_i * G_i) / \sum_{i=1}^{n} C_i$$

Where $\mathbf{C_i}$ is the number of credits of the i^{th} course and $\mathbf{G_i}$ is the grade point scored by the student in the i^{th} course and **n** is the number of courses registered in that semester.

ii) The CGPA is calculated in the same manner taking into account all the courses m, registered by a student over all the semesters of a programme, i.e., upto and inclusive of $\mathbf{S_k}$, where $k \geq 2$.

$$CGPA = \sum_{i=1}^{m} (C_i * G_i) / \sum_{i=1}^{m} C_i$$

iii) The SGPA and CGPA shall be rounded off to 2 decimal points.

12. **Award of Class:** After a student satisfies all the requirements prescribed for the completion of the Degree and becomes eligible for the award of M.Tech. Degree by JNTUH, he/she shall be placed in one of the following four classes:

S. No	Class Awarded	CGPA Secured
1	First Class with Distinction	CGPA ≥ 7.75
2	First Class	CGPA ≥ 6.75 and CGPA < 7.75
3	Second Class	CGPA ≥ 6.00 and CGPA < 6.75

Equivalence of grade to marks

Marks % = (CGPA -0.75)*100

13. **Withholding of Results:** If the student has not paid dues to the Institute/ University, or if any case of indiscipline is pending against him, the result of the student (for that Semester) may be withheld and he will not be allowed to go into the next Semester. The award or issue of the Degree may also be withheld in such cases.

14. **Re-Admission/Re-Registration (Re-Admission for Discontinued Student)**

- A student, who has discontinued the M. Tech. degree programme due to any reason whatsoever, may be considered for 'readmission' into the same degree programme (with the same specialization) with the academic regulations of the batch into which he gets readmitted, with prior permission from the authorities concerned.
- If a student is detained in a subject (s) due to shortage of attendance in any semester, he/she may be

  permitted to re-register for the same subject(s) in the same category (core or elective group) or equivalent subject, if the same subject is not available, as suggested by the Board of Studies of that department, as and when offered in the subsequent semester(s), with the academic regulations of the batch into which he/she seeks re-registration, with prior permission from the authorities concerned

- A candidate shall be given only one-time chance to re-register and attend the classes for a maximum of two subjects in a semester, if the internal marks secured by a candidate are less than 40% and failed in those subjects but fulfilled the attendance requirement. A candidate must re-register for failed subjects within four weeks of commencement of the class work, in the next academic year and secure the required minimum attendance. In the event of the student taking this chance, his Continuous Internal Evaluation (internal) marks and Semester End Examination marks obtained in the previous attempt stand cancelled.

15. **Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/Universities:** Transfer of students from the Constituent Colleges of JNTUH or from other Colleges/Universities shall be considered only on case-to-case basis by the Academic Council of the Institute.
16. **Transitory Regulations:** Students who have discontinued or have been detained for want of attendance, or who have failed after having undergone the PG degree Programme, may be considered eligible for readmission to the same or equivalent subjects as and when they are offered.
17. **General Rules**
    - **a)** The academic regulations should be read as a whole for the purpose of any interpretation.
    - **b)** In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Academic Council is final.
    - **c)** In case of any error in the above rules and regulations, the decision of the Academic Council is final.
    - **d)** The college may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the college.

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M. Tech (VLSI) - GR22 Course Structure

I M. Tech (VLSI) - I Semester

S.No	BOS	Group	Course Code	Course Name	Credits				Hours				Int.	Ext	Total Marks
					L	T	P	Total	L	T	P	Total			
1	ECE	PC	GR22D5071	Digital System Design using HDL	3	0	0	3	3	0	0	3	40	60	100
2	ECE	PC	GR22D5072	Digital CMOSIC Design	3	0	0	3	3	0	0	3	40	60	100
3	ECE	PE I		Professional Elective-I	3	0	0	3	3	0	0	3	40	60	100
4	ECE	PE II		Professional Elective-II	3	0	0	3	3	0	0	3	40	60	100
5	ECE	PC	GR22D5079	HDL Simulation Lab	0	0	2	2	0	0	4	4	40	60	100
6	ECE	PC	GR22D5080	Digital CMOS IC Design Lab	0	0	2	2	0	0	4	4	40	60	100
7	ENG	PC	GR22D5011	Research Methodology and IPR	2	0	0	2	2	0	0	2	40	60	100
TOTAL					**16**	**0**	**4**	**18**	**16**	**0**	**8**	**24**	**320**	**480**	**800**
8		AC		Audit Course I	0	0	0	0	2	0	0	2	40	60	100

PROFESSIONAL ELECTIVE – I				
S. No.	BOS	Group	Course Code	Course
1	ECE	PE	GR22D5073	Advanced Computer Architecture
2	ECE	PE	GR22D5074	Nano Fabrication and Wafer Technology
3	ECE	PE	GR22D5075	Scripting Languages for VLSI

PROFESSIONAL ELECTIVE – II				
S. No.	BOS	Group	Course Code	Course
1	ECE	PE	GR22D5076	Device Modeling
2	ECE	PE	GR22D5077	Internet of Things (IoT)
3	ECE	PE	GR22D5078	Hardware Software Co Design

I M. Tech (VLSI) - II Semester

S.No	BOS	Group	Course Code	Course Name	Credits				Hours				Int.	Ext	Total Marks
					L	T	P	Total	L	T	P	Total			
1	ECE	PC	GR22D5081	Analog CMOS IC Design	3	0	0	3	3	0	0	3	40	60	100
2	ECE	PC	GR22D5082	ASIC Design	3	0	0	3	3	0	0	3	40	60	100
3	ECE	PE III		Professional Elective-III	3	0	0	3	3	0	0	3	40	60	100
4	ECE	PE IV		Professional Elective-IV	3	0	0	3	3	0	0	3	40	60	100
5	ECE	PC	GR22D5089	Analog CMOSIC Design Lab	0	0	2	2	0	0	4	4	40	60	100
6	ECE	PC	GR22D5090	ASIC Design Lab	0	0	2	2	0	0	4	4	40	60	100
7	ECE	PW	GR22D5144	Mini Project	0	0	2	2	0	0	4	4	50	50	100
TOTAL					**14**	**0**	**6**	**18**	**14**	**0**	**12**	**26**	**320**	**480**	**800**
8		AC		Audit Course II	0	0	0	0	2	0	0	2	40	60	100

PROFESSIONAL ELECTIVE – III				
S. No.	BOS	Group	Course Code	Course
1	ECE	PE	GR22D5083	Micro-Electro- Mechanical Systems (MEMS) Design
2	ECE	PE	GR22D5084	System on Chip Architecture
3	ECE	PE	GR22D5085	Design for Testability

PROFESSIONAL ELECTIVE – IV				
S. No.	BOS	Group	Course Code	Course
1	ECE	PE	GR22D5086	Digital Signal Processors and Architecture
2	ECE	PE	GR22D5087	CAD for VLSI
3	ECE	PE	GR22D5088	Low Power VLSI Design

II M. Tech (VLSI) - I Semester

S.No	BOS	Group	Course Code	Course Name	Credits				Hours				Int.	Ext	Total Marks
					L	T	P	Total	L	T	P	Total			
1		PE V		Professional Elective-V	3	0	0	3	3	0	0	3	40	60	100
2		OE		Open Elective	3	0	0	3	3	0	0	3	40	60	100
3	ECE	PW	GR22D5145	Dissertation Phase – I	0	0	10	10	0	0	20	20	100		100
TOTAL					**6**	**0**	**10**	**16**	**6**	**0**	**26**	**26**	**180**	**120**	**300**

PROFESSIONAL ELECTIVE – V				
S. No.	BOS	Group	Course Code	Course
1	ECE	PE	GR22D5091	CPLD and FPGA architectures
2	ECE	PE	GR22D5092	VLSI Signal Processing
3	ECE	PE	GR22D5093	CMOS Mixed Signal Circuit Design

OPEN ELECTIVE				
S. No.	BOS	Group	Course Code	Course
1	CE	OE	GR22D5147	Cost Management of Engineering Projects
2	EEE	OE	GR22D5148	Industrial Safety
3	ME	OE	GR22D5149	Operations Research
4	ECE	OE	GR22D5150	Artificial Neural Networks and Fuzzy Systems
5	CSE	OE	GR22D5151	Cyber Security
6	IT	OE	GR22D5152	Internet of Things Architecture and Design Principles

II M. Tech (VLSI) - II Semester

S.No	BOS	Group	Course Code	Course Name	Credits				Hours				Int.	Ext	Total Marks
					L	T	P	Total	L	T	P	Total			
1	ECE	PW	GR22D5146	Dissertation Phase – II	0	0	16	16	0	0	32	32	100	100	200
TOTAL					**0**	**0**	**16**	**16**	**0**	**0**	**32**	**32**	**100**	**100**	**200**

Audit Courses I & II

1	GR22D5153	English for Research Paper Writing
2	GR22D5154	Disaster Management
3	GR22D5155	Sanskrit for Technical Knowledge
4	GR22D5156	Value Education
5	GR22D5157	Indian Constitution
6	GR22D5158	Pedagogy Studies
7	GR22D5159	Stress Management by Yoga
8	GR22D5160	Personality Development through Life Enlightenment Skills

I YEAR
I SEMESTER

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DIGITAL SYSTEM DESIGN USING HDL

Course Code: GR22D5071 **L/T/P/C: 3/0/0/3**
I Year I Semester

Course Objectives:
1. Learn digital design flow and Hardware generation in Verilog HDL.
2. To understand the Verilog HDL concepts.
3. To analyze and design Combinational Circuits in Verilog HDL.
4. To understand and design sequential circuits in Verilog HDL.
5. To design multipliers and processors.

Course Outcomes:
1. Create understanding of the digital design and techniques of Hardware generation in Verilog.
2. Create understanding of the fundamental concepts of Verilog HDL.
3. Learn implementation of Combinational Circuits in Verilog HDL.
4. Develop skills in modeling sequential circuits in Verilog HDL.
5. Develop skills in modeling multipliers and processors.

UNIT I
DIGITAL SYSTEM DESIGN AUTOMATION AND RTL DESIGN WITH VERILOG Digital Design Flow-design entry, Test bench in Verilog, Design validation, Compilation and synthesis, Post synthesis simulation, Timing analysis, Hardware generation in Verilog, Test Benches.

UNIT II
VERILOG LANGUAGE CONCEPTS Characterizing Hardware Languages, Module Basics, Verilog Simulation Model, Compiler Directives, System TASKs and Functions

UNIT III
Combinational Circuit Description Module Wires, Gate Level Logic, Hierarchical Structures, Describing Expressions with Assign statements, Behavioral Combinational Descriptions, Combinational Synthesis

UNIT IV
SEQUENTIAL CIRCUIT DESCRIPTION Sequential models, Basic Memory Components, Functional Registers, State Machine Coding, Sequential Synthesis. Component Test, Verification and Detailed Modeling.Test Bench, Test Bench Techniques, design Verification, Assertion Verification, Text Based Test Benches, Detailed Modeling- Switch Level Modeling, Strength Modeling

UNIT V
RTL DESIGN AND TEST Sequential Multiplier- Shift-and- Add Multiplication process, sequential multiplier design, Multiplier testing, Von Neumann Computer Model- Processor and memory model, processor model specification, designing the adding CPU, Design of data path, Control part design, Adding CPU verilog description, testing adding CPU.

Text Books

1. Zainalabdien Navabi, Verlog Digital System Design, TMH, 2nd edition.

Reference Books:

1. Fundamentals of Digital Logic with Verilog design by Stephen. Brown and Zvonko Vranesis, TMH, 2nd edition2010.
2. Digital Logic Design using Verilog, State machine & synthesis for FPGA, Sunggulee, Cengage Learning, 2009
3. Verilog HDL- SamirPalnitkar, 2nd edition.
4. Advanced Digital Design with Verilog HDL- Michael D. Ciletti, PHI, 2005.
5. Digital Systems Design using VHDL- Charles H Roth, Jr. Thomson Publications, 2004

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DIGITAL CMOS IC DESIGN

Course Code: GR22D5072 **L/T/P/C: 3/0/0/3**
I Year I Semester

Course Objectives:
1. To understand the evolution of CMOS integrated circuits.
2. To develop design ability of combinational MOS logic circuits
3. To design the ability of sequential MOS logic circuits.
4. To appreciate and design dynamic logic circuits.
5. To design semiconductor memories based on MOS

Course Outcomes:
1. An ability to analyze the Pseudo NMOS and CMOS logic families
2. An ability to design combinational MOS logic circuits.
3. An ability to design sequential MOS logic circuits.
4. An ability to design dynamic MOS logic circuits.
5. Able to design semiconductor memories.

UNIT I
MOS DESIGN Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Transistor equivalency, Power dissipation, CMOS Inverter logic.

UNIT II
COMBINATIONAL MOS LOGIC CIRCUITS Pseudo NMOS logic gates, MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT III
SEQUENTIAL MOS LOGIC CIRCUITS Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT IV
DYNAMIC LOGIC CIRCUITS Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT V
SEMICONDUCTOR MEMORIES Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Text Books

1. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 4rd Ed., 2016.

Reference Books

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
ADVANCED COMPUTER ARCHITECTURE
(PROFESSIONAL ELECTIVE I)

Course Code: GR22D5073 **L/T/P/C: 3/0/0/3**
I Year I Semester

Course Objectives:
1. To learn how to build the best processor/computing system understanding the underlying tradeoffs and ramifications.
2. To identify and analyze the attributes of computer architecture design with recent trend technology.
3. To identify the techniques to improve the speed and performance of computers
4. Parallelism in Instruction level – Hardware approaches – pipelining, dynamic scheduling, superscalar processors, and multiple issue of instructions.
5. To implement the design aspects and categorize various issues, causes and hazards due to parallelisms.

Course Outcomes:
1. An ability to discuss the organization of computer-based systems and how a range of design choices are influenced by applications.
2. An ability to understand the components and operation of a memory hierarchy and the range of performance issues influencing its design.
3. An ability to interpret the organization and operation of current generation parallel computer systems, including multiprocessor and multi core systems.
4. An ability to understand the various techniques to enhance a processors ability to exploit instruction-level parallelism (ILP), and its challenges.
5. An ability to undertake performance comparisons of modern and high performance computers.

UNIT I
FUNDAMENTALS OF COMPUTER DESIGN
Fundamentals of Computer design, Changing faces of computing and TASK of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, Quantitative principles of computer design, Amdahl‟s law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing type and size of operands, Operations in the instruction set.

UNIT II
PIPELINES Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties. Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT III
INSTRUCTION LEVEL PARALLELISM (ILP) - THE HARDWARE APPROACH
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo‟s approach, Branch prediction, High performance instruction delivery- Hardware based speculation.

ILP Software Approach:
Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware verses Software.

UNIT IV
MULTI PROCESSORS AND THREAD LEVEL PARALLELISM
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT V
INTER CONNECTION AND NETWORKS
Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

Text Books
1. John L. Hennessy, David A. Patterson - Computer Architecture: A Quantitative Approach, 3rd Edition, an Imprint of Elsevier.

Reference Books
1. John P. Shen and Miikko H. Lipasti -, Modern Processor Design : Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing - Kai Hwang, Faye A.Brigs., MC Graw Hill.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
NANO FABRICATION AND WAFER TECHNOLOGY
(PROFESSIONAL ELECTIVE I)

Course Code: GR22D5074 **L/T/P/C: 3/0/0/3**
I Year I Semester

Course Objective:
1. To provide students with a glimpse into the semiconductor industry
2. To provide insight into the future of that industry as well as nanotechnology
3. The dimensions of the features built into integrated circuits in general
4. The dimensions of the features built into integrated circuits when approach atomic dimensions,
5. To provide students with nanotechnology challenges and opportunities.

Course Outcomes:
1. The students will be exposed to state-of-the-art VLSI process technologies.
2. Student will also become more familiar with the relevant diagnostic techniques for process related issues.
3. Students will be equipped with a basic understanding of the Oxidation, Lithography, and deposition techniques.
4. Students will be familiarized with various etching techniques of CMOS, and can visualize various etch models.
5. Visualize the steps taken for MOS fabrication technologies.

UNIT I
INTRODUCTION TO NANOFABRICATION
Semiconductor materials, Environment for VLSI Technology: Clean room and safety requirements, Single crystal growth (Technique), Crystal defects., Wafer cleaning processes and wet chemical etching techniques, Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterization of Impurity profiles.

UNIT II
OXIDATION Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterization of oxide films; High k and low k dielectrics for ULSI.

UNIT III
LITHOGRAPHY Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

UNIT IV
DEPOSITION TECHNIQUES: Chemical Vapor Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.
Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallization schemes.

UNIT V

ETCHING AND PROCESS INTEGRATION

Dry etching: Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI

Wet etching: Wet Etching and Basic Concepts, wet etchants, selectivity, Isotropic and anisotropic etching profile. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technologies.

Text Books:

1. Silicon VLSI Technology: Fundamentals, Practice, and Modeling," James D. Plummer, Michael D C.Y. Chang and S.M.Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.
2. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.
3. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.

References:

1. Semiconductor Materials and Device Characterization, Dieter K.Schroder, Wiley Interscience
2. The science and engineering of microelectronic fabrication, Stephen A. Campbell, Oxford, 2001
3. Semiconductor Lithography Principles, practice and materials, Wayne M. Moreau, Plenum Press

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
SCRIPTING LANGUAGES FOR VLSI
(PROFESSIONAL ELECTIVE I)

Course Code: GR22D5075 **L/T/P/C: 3/0/0/3**
I Year I Semester

Course Objectives:
1. To describe the need of using scripting language programs.
2. To use PERL scripting language at the instances required.
3. To apply advanced level PERL for software automation.
4. To employ the PERL scripting language for file system navigation.
5. To illustrate software automation using TCL

Course Outcomes:
1. The students will be in a position to judge whether scripting language program is needed for a particular code.
2. Students will be acquainted with the basic level scripting language programming in PERL.
3. Students will be skillful to code in PERL for advanced level software automation.
4. Students will have the programming skills to automate the software for event- driven programs too.
5. Students will be in a position to demonstrate software automation using Java Script, PERL TK, and in basic level using python scripting language.

UNIT I
INTRODUCTION TO SCRIPTS AND SCRIPTING
Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT II
ADVANCED PERL Finer points of looping, subroutines, using pack and unpack, working with files, navigating the file system, type globs, eval, references, data structures, packages, libraries and modules, objects, objects and modules in action, tied variables, interfacing to the operating systems, security issues**.**

UNIT III
TCL:The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT IV
ADVANCED TCLThe eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and- bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT V

TK AND JAVASCRIPT: Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK. JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Python. Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

Text Books:

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference- Herbert Schildt, 7th Edition, TMH.

Reference Books:

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann SerieS.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DEVICE MODELING
(PROFESSIONAL ELECTIVE II)

Course Code: GR22D5076 **L/T/P/C: 3/0/0/3**
I Year I Semester

Course Objectives
1. To impart to students knowledge of semi conductor physics and integrated passive devices.
2. To enable students to analyze the behavior of monolithic diodes with the help of models of integrated diodes.
3. To enable students to analyze the behavior of integrated NMOS and PMOS transistors with the help of SPICE models.
4. To enable students visualize different VLSI fabrication techniques of different processes.
5. To enable students to model hetero junction devices.

Course Outcomes
1. The graduate student will be equipped with knowledge of semiconductor physics.
2. The graduate student will be able relate model parameters to structures of integrated passive devices.
3. The graduate will be able to analyze static and dynamic behavior of diodes.
4. The graduate student will be able to model electrically NMOS and PMOS transistors.
5. The graduate student will be able to use SPICE model level 1, 2,3and 4 and hence will be able to analyze various integrated circuits.

UNIT I
INTRODUCTION TO SEMICONDUCTOR PHYSICS
Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation.
Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT II
INTEGRATED DIODES Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models
Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT III
INTEGRATED MOS TRANSISTOR NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT IV
VLSI FABRICATION TECHNIQUES An overview of wafer fabrication, Wafer Processing – Oxidation –Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p- well- twin tub- Silicon on insulator – CMOS process enhancements –Interconnects circuit elements

UNIT V

MODELING OF HETERO JUNCTION DEVICES Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

Text Books:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

Reference Books:

1.Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
INTERNET OF THINGS
(PROFESSIONAL ELECTIVE II)

Course Code: GR22D5077 **L/T/P/C: 3/0/0/3**
I Year I Semester

Course Objectives:
1. Understand the basic characteristics of IoT system
2. Realize the different IoT Protocols architectures
3. Analyze the cloud interface and security concerns of IoT devices
4. Introduce programming in various real-time hardware platforms
5. Design a complete IoT ecosystem for various smart applications

Course Outcomes:
1. Ability to learn characteristics, applications, components and challenges of Internet of Things (IOT)
2. Create understanding of IOT networking concepts – terminologies, stack components infrastructure and data protocols
3. Create understanding of the concept of Cloud for IOT challenges, cloud service providers and security aspects
4. Develop skills in understanding and programming the Arduino and Raspberry Pi hardware platforms
5. Make the student understand the requirements, components and challenges involved in specific IOT application areas - smart homes, grids and cities and industrial IOT

UNIT I
INTRODUCTION TO IOT Characteristics of IOT, Applications of IOT, IOT Categories, IOT Enablers and Connectivity Layers, Sensors, Actuators, IOT Components & Implementation, Challenges for IOT.

UNIT II
IOT NETWORKING & CONNECTIVITY TECHNOLOGIES
Connectivity terminologies-IOT Node, LAN,WAN, Gateway, IOT Stack vs. Web Stack, IOT Identification and Data Protocols-IPV4,IPV6,HTTP,MQTT,COAP, Connectivity Technologies – Zigbee, Bluetooth, LoRa

UNIT III
CLOUD FOR IOT IOT with Cloud-Challenges, Cloud service providers for IOT-Overview, Cloud Computing – Security aspects, Case Study.

UNIT IV
HARDWARE PLATFORMS Programming with Arduino-Features of Arduino, Components of Arduino Board, Arduino IDE, Program Elements, Raspberry Pi – Introduction, Architecture, PIN Configuration, Implementation of IOT with Raspberry Pi

UNIT V
IOT APPLICATIONS Smart Homes-Smart Home Origin, Technologies, Implementation, Smart Grids-Characteristics, Benefits, Architecture, Components, Smart Cities-Characteristics,

Frameworks, Challenges, Industrial IOT- Requirements, Design Considerations, Applications.

Text Books:

1. Internet of Things, Jeeva Jose, Khanna Publishing, 2018
2. Internet of Things, Abhishek S Nagarajan, RMD Sundaram, Shriram K Vasudevan, Wiley, 2019

Reference Books:

1. The Internet of Things, Michael Miller, Pearson Education Limited, 2015
2. Internet of Things: Architecture, Implementation and Security, Mayur Ramgir, Pearson Education Limited, 2019
3. IOT Fundamentals: Networking Technologies, Protocols and Use Cases for IOT, Rowan Trollope, David Hanes, Patrick Gassetete, Jerome Henry,Pearson Education Limted, 2017
4. Beginning LoRa Radio Networks with Arduino, Pradeeka Seneviratne, Apress, 2019

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
HARDWARE AND SOFTWARE CO-DESIGN
(PROFESSIONAL ELECTIVE II)

Course Code: GR22D5078 **L/T/P/C: 3/0/0/3**
I Year I Semester

Course Objectives:
1. Analyze and explain the control-flow and data-flow of a software program and a cycle-based hardware description,
2. Transform simple software programs into cycle-based hardware descriptions with equivalent behavior and vice versa,
3. Partition simple software programs into hardware and software components, and create appropriate -hardware-software interfaces to reflect this partitioning,
4. Identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components, and
5. Use simulation software to co-simulate software programs with cycle-based hardware descriptions.

Course Outcomes:
1. To acquire the knowledge on various models of Co-design.
2. To explore the interrelationship between Hardware and software in a embedded system
3. To acquire the knowledge of firmware development process and tools during Co-esign.
4. Understand validation methods and adaptability.
5. to get familiarity with the soft wares for simulation and co-simulation

UNIT I
Co- Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.Co- Synthesis Algorithms: Hardware software synthesis algorithms: hardware – softwarepartitioning distributed system co-synthesis.

UNIT II
Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure. Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems(8051-Architectures for High performance control), Architecture for Data dominated systems(ADSP21060, TMS320C60), Mixed Systems.

UNIT III
Compilation Techniques and Tools for Embedded Processor Architectures: Modern embeddedarchitectures, embedded software development needs, compilation technologies, practicalconsideration in a compiler development environment.

UNIT IV
Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,Languages for System – Level Specification and Design-II: Heterogeneous specifications andmulti-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS/REFERENCES:

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.
2. Hardware / Software Co- Design - Giovanni De Micheli, MariagiovannaSami, Kluwer Academic Publishers, 2002.
3. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer,2010

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
HDL SIMULATION LAB

Course Code: GR22D5079 **L/T/P/C: 0/0/4/2**
I Year I Semester

Course Objectives:
1. To impart the knowledge on design of digital circuits using HDL with example digital circuits.
2. To enable the students to design combinational and sequential logic circuits using VHDL language.
3. To impart the knowledge of Verilog language to design digital circuit in behavioral, dataflow and structural model
4. To enable the students to synthesize the digital and sequential circuits and analyze them.
5. To demonstrate the functionality of digital circuits using various fault models.

Course Outcomes:
1. Interpret the HDL design styles, data types to implement the basic digital circuits.
2. Analyze the basic logic circuits in Xilinx tool.
3. Apply the HDL knowledge to implement combinational and sequential digital circuits.
4. Make use of the Xilinx tool Knowledge to synthesis the combinational and sequential circuits.
5. Test for the functionality of digital circuit by using various fault models

Note: All the following digital circuits are to be designed and implemented on FPGA using XILINX‟s/ Altera‟s/ Equivalent CAD tools.
Programming can be done using any HDL compiler, Verification of the Functionality of the module using functional Simulator, Timing Simulator for Critical Path tine Calculation, Synthesis of module, Place & Route and implementation of design using FPGA.

TASK 1
Design of primitive elements using Verilog/ VHDL

TASK 2
Implementation of Digital Circuits using Verilog/ VHDL

TASK 3
Design of arithmetic circuits using Verilog/ VHDL

TASK 4
Verification of the Functionality of designed Circuits using function Simulator.

TASK 5
Timing Simulation for critical path time calculation.

TASK 6
Synthesis of Digital Circuits.

TASK 7

Place and Route techniques for major FPGA vendors such as Xilinx/ Altera/ Actel etc.

TASK 8

Implementation of Designed Digital Circuits using FPGA and CPLD devices.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DIGITAL CMOS IC DESIGN LAB

Course Code: GR22D5080 **L/T/P/C: 0/0/4/2**
I Year I Semester

Course Objectives:
1. To describe over view about evolution of CMOS integrated circuits.
2. To provide knowledge about Combinational, Sequential MOS logic circuits
3. To introduce and familiarize with the various logic circuits.
4. To prepare them to face the challenges in dynamic logic circuits.
5. To prepare them to design various building blocks in combinational and sequential circuits.

Course Outcomes:
1. An ability to know about the various Combinational and Sequential MOS logic circuits.
2. An in-depth knowledge of applying the concepts on real time applications
3. An ability to understand the basic concepts of Boolean expressions.
4. Able to design different Combinational logic blocks.
5. Able to analyze and implement various memory elements.

TASK 1
For a given specifications plot the characteristics for NMOS and PMOS transistors by varying ID, VDS and VGS.

TASK 2
For a given specifications plot VTC Curve for CMOS Inverter and calculate $V_{IL,}$ VIH, NMH, NML.

TASK 3
For a given specifications plot VTC Curve for CMOS Inverter with varying VDD

TASK 4
For a given specifications plot VTC Curve for CMOS Inverter with varying Device size.

TASK 5
Perform transient of CMOS inverter with no0 load and with load and determine TPHL, TPHL.

TASK 6
Design and Draw layout for CMOS NOR/ NAND gate and perform DRC, LVS, RC Extraction.

TASK 7
Design and Draw layout for CMOS XOR gate using Transmission Gates and perform DRC, LVS, RC Extraction.

TASK 8
Design and Draw layout for combinational function using CMOS logic and perform DRC, LVS, RC Extraction.

TASK 9

Design and Draw layout for D- Flip Flop using CMOS logic and perform DRC, LVS, RC Extraction.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
RESEARCH METHODOLOGY AND IPR

Course Code: GR22D5011 **L/T/P/C: 2/0/0/2**
I Year I Semester

Course Objectives:
1. To familiarize students with the different aspects of research.
2. To provide an idea of good scientific writing and proper presentation skills.
3. To provide an understanding of philosophical questions behind scientific research.
4. To provide a brief background on the historical legacy of science.
5. To Provide an insight of nature of Intellectual Property and new developments in IPR.

Course Outcomes:
1. Understand research problem formulation and analyze research related information and follow research ethics.
2. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
3. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasize the need of information about Intellectual Property Right to be promoted among students in general & engineering.
4. Understand the nature of Intellectual Property and IPR in International scenario.
5. Understand that IPR protection provides an incentive to inventors for further and design the administration of patent system and new Developments in IPR.

UNIT I
Research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNITII
Effective literature studies approaches, analysis Plagiarism, Research ethics, Citation

UNIT III
Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT IV
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNITV
New Developments in IPR: Administration of Patent System.New developments in IPR; IPR of Biological Systems, Computer Software etc.Traditional knowledge Case Studies, IPR and IITs.

Text books and references:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by StepGuidefor beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
5. Mayall, "Industrial Design", McGraw Hill, 1992.
6. Niebel, "Product Design", McGraw Hill, 1974.
7. Asimov, "Introduction to Design", Prentice Hall, 1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016

I YEAR
II SEMESTER

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
ANALOG CMOS IC DESIGN

Course Code: GR22D5081 **L/T/P/C: 3/0/0/3**
I Year II Semester

Course Objectives:
1. To model MOS devices and .integrated passive components.
2. To analyze CMOS sub-circuits.
3. To analyze and design various amplifiers &operational amplifiers.
4. To study in deep various configurations of operational amplifiers.
5. To design various comparators and to characterize comparators.

Course Outcomes
1. Develop model MOS devices and .integrated passive components.
2. Design circuits using CMOS sub-circuits.
3. Design amplifiers and operational amplifiers for real time applications.
4. Design circuits based on various configurations of operational amplifiers.
5. Develop applications of CMOS operational amplifier based comparators.

UNIT I
MOS DEVICES AND MODELING
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT II
ANALOG CMOS SUB-CIRCUITS
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT III
CMOS AMPLIFIERS
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT IV
CMOS OPERATIONAL AMPLIFIERS
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT V
COMPARATORS
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Text Books:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

Reference Books:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
ASIC DESIGN

Course Code: GR22D5082 **L/T/P/C: 3/0/0/3**
I Year II Semester

Course Objectives:
1. To understand the ASICs and CMOS logic.
2. To know in detail about programmable ASICs and its interconnects.
3. To understand about programmable ASIC its logic synthesis, simulation and testing of VLSICircuits
4. To understand about Interconnects and design software
5. To know in detail about physical design flow

Course Outcomes:
1. Ability to apply logical effort technique for predicting delay, delay minimization and understand ASIC Design flow
2. Gain knowledge to design logic cells and I/O cells
3. Categorize different types of ASICs and explain their technology
4. Evaluate the algorithms for floor planning and placement of cells and to apply routing algorithms for optimization of length and speed.
5. Analysis the concept of routing techniques

UNIT I
INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY
Types of ASICs, Design flow, CMOS transistors, Combinational Logic Cell, Sequential logic cell, Data path logic cell , Transistors as Resistors & Transistor Parasitic Capacitance, Logical effort

UNIT II
LOGIC CELLS AND I/O CELLS
Anti fuse, Static RAM, EPROM and EEPROM technology, Xilinx LCA, Altera FLEX-AlteraMAX, DC & AC outputs, DC & AC inputs, Clock & Power inputs, Xilinx I/O blocks

UNIT III
INTERCONNECT AND DESIGN SOFTWARE
Xilinx LCA-Xilinx EPLD, Altera MAX 5000,7000,9000, Altera FLEX, Design systems, Half gate ASIC, Schematic entry, Low level design language, PLA tools-EDIF

UNIT IV
LOGIC SIMULATION, SYNTHESIS AND PARTITIONING
Types of simulation, Verilog and logic synthesis, , System partition, FPGA partitioning, Partitioning Methods, Examples Constructive and Iterative, Portioning, K-L Algorithms.

UNIT V
PHYSICAL DESIGN
Physical design flow, - Floor planning - Placement -– Global routing - Detailed routing - Circuit extraction – DRC.

Text Books:

1. M.J.S .Smith, "Application Specific Integrated Circuits", Pearson Education, 2010.
2. Farzad Nekoogar and FaranakNekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.
3. D. Papa, I. Markov. "Multi-Objective Optimization in Physical Synthesis of Integrated Circuits" Springer; 2012.
4. V.Taraate, "Digital Logic Design Using Verilog: Coding and RTL Synthesis", Springer; 2016.

Reference Books:

1. G.Hachtel, F. Somenzi. Logic Synthesis and Verification Algorithms. Springer; 2013
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
MICRO-ELECTRO-MECHANICAL SYSTEMS (MEMS) DESIGN
(PROFESSIONAL ELECTIVE III)

Course Code: GR22D5083 **L/T/P/C: 3/0/0/3**
I Year II Semester
Course Objective:
1. To provide knowledge of semiconductors and solid mechanics to fabricate MEMS devices.
2. To educate on the rudiments of Micro fabrication techniques.
3. To introduce various sensors and actuators
4. To introduce different materials used for MEMS
5. To educate on the applications of MEMS to disciplines beyond Electrical and Mechanical engineering.

Course Outcomes:
1. Ability to understand the operation of micro devices, micro systems and their applications.
2. Ability to design the micro devices, micro systems using the MEMS fabrication process.
3. Student will be able to appreciate the role of MEMS sensors and actuators in your daily life. Being able to explain "Why we should care about these devices?"
4. Student will understand the role of the MEMS design and trade-offs in real world.
5. Student will understand the MEMS fabrication process, design and packaging

UNIT I
INTRODUCTION
Intrinsic Characteristics of MEMS – Energy Domains and Transducers- Sensors and Actuators – Introduction to Micro fabrication - Silicon based MEMS processes – New Materials – Review of Electrical and Mechanical concepts in MEMS – Semiconductor devices – Stress and strain analysis – Flexural beam bending- Torsional deflection.

UNIT II
SENSORS AND ACTUATORS-I
Electrostatic sensors – Parallel plate capacitors – Applications – Interdigitated Finger capacitor – Comb drive devices – Micro Grippers – Micro Motors – Thermal Sensing and Actuation – Thermal expansion – Thermal couples – Thermal resistors – Thermal Bimorph – Applications – Magnetic Actuators – Micromagnetic components – Case studies of MEMS in magnetic actuators- Actuation using Shape Memory Alloys.

UNIT III
SENSORS AND ACTUATORS-II
Piezoresistive sensors – Piezoresistive sensor materials – Stress analysis of mechanical elements – Applications to Inertia, Pressure, Tactile and Flow sensors – Piezoelectric sensors and actuators – piezoelectric effects – piezoelectric materials – Applications to Inertia , Acoustic, Tactile and Flow sensors.

UNIT IV
MICROMACHINING
Silicon Anisotropic Etching – Anisotrophic Wet Etching – Dry Etching of Silicon – Plasma Etching – Deep Reaction Ion Etching (DRIE) – Isotropic Wet Etching – Gas Phase Etchants – Case studies –Basic surface micro machining processes – Structural and Sacrificial Materials – Acceleration of sacrificial Etch – Striction and Antistriction methods – LIGA Process -

Assembly of 3D MEMS – Foundry process.

UNIT V
MICROSYSTEMS DESIGN AND PACKAGING

Design considerations, Mechanical Design, Process design, Realization of MEMS components using intellisuite. Micro system packaging, Packing Technologies, Assembly of Microsystems, Reliability in MEMS.

Text Book:

1. Chang Liu, 'Foundations of MEMS', Pearson Education Inc., 2012.
2. Stephen D Senturia, 'Microsystem Design', Springer Publication, 2000.
3. Tai Ran Hsu, "MEMS & Micro systems Design and Manufacture" Tata McGraw Hill, New Delhi, 2002.

Reference Books:

1. Nadim Maluf," An Introduction to Micro Electro Mechanical System Design", Artech House, 2000.
2. Mohamed Gad-el-Hak, editor, " The MEMS Handbook", CRC press Baco Raton, 2001.
3. Julian w. Gardner, Vijay K. Varadan, Osama O.Awadelkarim, Micro Sensors MEMS and Smart Devices, John Wiley & Son LTD, 2002.
4. James J.Allen, Micro Electro Mechanical System Design, CRC Press Publisher, 2005.
5. Thomas M.Adams and Richard A.Layton, "Introduction MEMS, Fabrication and Application," Springer, 2010.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
SYSTEM ON CHIP ARCHITECTURE
(PROFESSIONAL ELECTIVE III)

Course Code: GR22D5084 **L/T/P/C: 3/0/0/3**
I Year II Semester

Course Objectives:
1. To describe the system design approach with respect to the hardware and software.
2. To apply the techniques for reducing the delays in program execution.
3. To categorize and compare different processor types for their selection into a System on Chip.
4. To compare different memory designs and their purposes
5. To interpret the architectures and applications of various buses.

Course Outcomes:
1. Students will be able to summarize all the components required for system design.
2. Students will be acquired the techniques to minimize the delays for better performance of a system on chip.
3. Students will be able to analyze different types of buses for respective applications.
4. Students will be skilful to judge a configurable device based on the application requirement for a system on chip
5. Students will have the technique to implement AES algorithm if required.

UNIT I
INTRODUCTION TO THE SYSTEM APPROACH
System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT II
PROCESSORS
Introduction ,Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III
MEMORY DESIGN FOR SOC
Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation ,SOC Memory System, Models of Simple Processor – memory interaction.

UNIT IV
INTERCONNECT CUSTOMIZATION AND CONFIGURATION
Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design,

Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT V
APPLICATION STUDIES / CASE STUDIES
SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG Compression.

Text Books:
1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional

Reference Books:
1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DESIGN FOR TESTABILITY
(PROFESSIONAL ELECTIVE III)

Course Code: GR22D5085 **L/T/P/C: 3/0/0/3**
I Year II Semester

Course Objectives
1. To understand basics of VLSI Testing.
2. To develop the knowledge of algorithms for fault simulation.
3. To provide knowledge on Testability Measures.
4. To develop knowledge of BIST architecture.
5. To train on Boundary Scan Test methodology.

Course Outcomes
1. Model faults and differentiate their levels.
2. Apply fault simulation algorithms.
3. Calculate Controllability and Observability measures for combinational and sequential circuits.
4. An ability to design the BIST architecture for a chip.
5. Apply Boundary Scan Standards during the development of chip.

UNIT I
INTRODUCTION TO TESTING
Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT II
LOGIC AND FAULT SIMULATION
Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT III
TESTABILITY MEASURES
SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT IV
BUILT-IN SELF-TEST
The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per- Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT V
BOUNDARY SCAN STANDARD
Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

Text Books:

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V. D. Agrawal, Kluwer Academic Pulishers.

Reference Books:

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE
(PROFESSIONAL ELECTIVE IV)

Course Code: GR22D5086 **L/T/P/C: 3/0/0/3**
I Year II Semester

Course Objectives:
1. To provide sound foundation of digital signal processing (DSP) architectures for designing efficient VLSI architectures for DSP systems.
2. To analyze general purpose digital signal processors.
3. To understand pipelining, parallel processing and retiming.
4. To illustrate the features of on-chip peripheral devices and its interfacing along with its programming details.
5. To analyze DSP architectures.

Course Outcomes:
1. An ability to recognize the fundamentals of fixed and floating point architectures of various DSPs.
2. An ability to learn the architecture details and instruction sets of fixed and floating point DSPs.
3. An ability to Infer about the control instructions, interrupts, and pipeline operations.
4. AnabilitytoanalyzeandlearntoimplementthesignalprocessingalgorithmsinDSPs.
5. An ability to learn the DSP programming tools and use them for applications.

UNIT I
INTRODUCTION TO DIGITAL SIGNAL PROCESSING
Introduction, a Digital signal-processing system, the sampling process, discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT II
COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS
Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III
ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES
Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation UNIT, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS
Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT V

ANALOG DEVICES FAMILY OF DSP DEVICES

Analog Devices Family of DSP Devices – ALU and MAC block diagram, Shifter Instruction, Base Architecture of ADSP 2100, ADSP-2181 high performance Processor. Introduction to Black fin Processor - The Black fin Processor, Introduction to Micro Signal Architecture,Overview of Hardware Processing UNITs and Register files, Address Arithmetic UNIT, Control UNIT, Bus Architecture and Memory, Basic Peripherals.

Text Books:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. APractical Approach To Digital SignalProcessing-K Padmanabhan,R. Vijayarajeswaran, Ananthi. S, New Age International, 2006/2009
3. Embedded Signal Processing with the Micro Signal Architecture: Woon-Seng Gan, Sen M. Kuo, Wiley-IEEE Press, 2007

Reference Books:

1. Digital Signal Processors, Architecture, Programming and Applications–B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
CAD FOR VLSI
(PROFESSIONAL ELECTIVE IV)

Course Code: GR22D5087 **L/T/P/C: 3/0/0/3**
I Year II Semester

Course Objectives:
1. To provide an introduction to the VLSI and Physical design cycle.
2. To study various physical design methods in VLSI.
3. To understand the concepts behind the various routing techniques.
4. To analyze physical design automation of FPGA's and MCM's.
5. To understand the concepts of chip input and output circuits.

Course Outcome:
1. Establish comprehensive understanding of the various CAD design cycles
2. Demonstrate knowledge and understanding of fundamental concepts in physical design.
3. An ability to know different routing techniques
4. Develop skills in understanding the physical design automation .
5. To gain knowledge on the methodologies involved in chip design.

UNIT I
VLSI PHYSICAL DESIGN AUTOMATION
VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles

UNIT II
PARTITIONING, FLOOR PLANNING, PIN ASSIGNMENT AND PLACEMENT
Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing, Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments, Placement – Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

UNIT III
GLOBAL ROUTING AND DETAILED ROUTING
Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT IV
PHYSICAL DESIGN AUTOMATION OF FPGAs
FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model. physical design automation of MCMs.Introduction to MCM Technologies, MCM Physical Design Cycle.

UNIT V
CHIP INPUT AND OUTPUT CIRCUITS

ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

Text Books:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
LOW POWER VLSI DESIGN
(PROFESSIONAL ELECTIVE IV)

Course Code: GR22D5088 **L/T/P/C: 3/0/0/3**
I Year II Semester

Course Objectives:

1. To know about the fundamentals and need for low power circuit design.
2. To furnish knowledge of various low power design approaches for VLSI System design.
3. To Understand the concepts of low voltage and low power design techniques for adders.
4. To Understand the concepts of low voltage and low power design techniques for multipliers
5. To analyze different low voltage low power memories using low power techniques.

Course Outcomes:

1. Understand the fundamentals of low power VLSI circuit design.
2. Build knowledge of various low power VLSI design approaches.
3. Design low voltage and low power data path subsystems such as adders.
4. Design low voltage and low power data path subsystems such as multipliers.
5. Analyze and design low voltage and low power memories

UNIT I
Fundamentals of Low Power
Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II
Low Power Design Approaches
Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT III
Low-Voltage Low-Power Adders
Introduction, Standard Adder Cells, CMOS Adder"s Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT IV
Low-Voltage Low-Power Multipliers
Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT V

Low-Voltage Low-Power Memories

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Text Books:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
ANALOG CMOS IC DESIGN LAB

Course Code: GR22D5089 **L/T/P/C: 0/0/4/2**
I Year II Semester

Course Objectives:
1. To describe over view about evolution of CMOS integrated circuits.
2. To introduce and familiarize with the various current mirrors
3. To provide knowledge about fabrication process and technology
4. To introduce and familiarize with the various Amplifiers & OP-amps
5. To prepare them to face the challenges in CMOS technology

Course Outcomes:
1. Able to develop an in-depth understanding of the design principles and applications of CMOS analog IC design.
2. An ability to know the fabrication steps involved in CMOS technology.
3. Familiar with the small signal and large signal models of CMOS transistors.
4. An in-depth knowledge of applying the concepts on real time applications.
5. Analyze and design of CMOS op Amps and compensation techniques.

TASK1
Analyze the NMOS and PMOS Operating point Characteristics.

TASK2
Design a Simple MOS Current Mirror and find out the AC, DC, OP analysis.

TASK3
Design a MOS Wilson current mirror and find out the AC, DC, OP analysis.

TASK4
Design a MOS cascode current mirror and find out the AC, DC, OP analysis.

TASK5
Design a NMOS Differential Amplifier and find out the AC, DC, OP analysis.

TASK6
Design a PMOS Differential Amplifier and find out the AC, DC, OP analysis.

TASK7
Design a CMOS Operational Amplifier and find out the AC analysis and noise margin analysis.

TASK8
Design a comparator using Operational Amplifier and find out the AC analysis.

TASK9

Draw the Analog Layout for CMOS current Mirror and perform DRC, LVS, RC Extraction.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
ASIC DESIGN LAB

Course Code: GR22D5090 **L/T/P/C: 0/0/4/2**
I Year II Semester

Course Objectives
1. To enable the students to explain the Basic VLSI physical design flow.
2. To enable the student to identify the various algorithms for partitioning, floor planning and Pin assignment.
3. To make the student to be able to differentiate between global routing and detailed routing.
4. To impart the knowledge on various algorithms for global and detailed routing.
5. To train the students to explain the physical design automation of FPGAs

Course Outcomes
1. At the end of the Course, Student will be able to:
2. Explain the VLSI physical Design automation
3. Apply Algorithms required for partitioning, floor planning, pin assignment and placement
4. Explain global and detailed routing, , RC extraction for given netlist to meet the specifications.
5. Demonstrate Physical design automation of FPGAs

TASK 1
Develop a Verification environment using system Verilog for any one digital system.

TASK 2
Design and analyze the performance with respect to area, power and speed for Ripple Carry Adders using ASIC Logic Design Tools.

TASK 3
Design and analyze the performance with respect to area, power and speed for Carry lookahead Adder using ASIC Logic Design Tools.

TASK 4
Design and analyze the performance with respect to area, power and speed for Array Multiplier using ASIC Logic Design Tools.

TASK 5
Design and analyze the performance with respect to area, power and speed for Wallace Multiplier using ASIC Logic Design Tools.

TASK 6
Perform Synthesis for any digital system to meet the given specifications.

TASK 7
Perform Static Timing Analysis for any digital system to meet the given specifications.

TASK 8

Perform Floor planning, , clock tree synthesis, Placement and Routing, RC extraction for given netlist to meet the specifications.

Note: All the following digital circuits are to be designed and implemented using Cadence/ Mentor Graphics/ Synopsys/ equivalent CAD Tools.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
MINI PROJECT

Course Code: GR22D5144 **L/T/P/C: 0/0/4/2**
I Year II Semester

Course Objectives:
1. To improve the technical presentation skills of the students.
2. To train the students to do literature review.
3. To impart critical thinking abilities for problem solutions.
4. To learn different implementation techniques.
5. To prepare technical reports

Course Outcomes:
1. Choose the problem domain in the specialized area under computer science and engineering.
2. Acquire and categorize the solution paradigms with help of case studies
3. Design and code using selected hardware, software and tools.
4. Execute, Implement and demonstrate the problem statement by using the selected hardware,software and tools.
5. Document the thesis and publish the final work in a peer reviewed journal.

Syllabus Contents:
Mini Project will have mid semester presentation and end semester presentation. Mid semester presentation will include identification of the problem based on the literature review on the topic referring to latest literature available.
End semester presentation should be done along with the report on identification of topic for the work and the methodology adopted involving scientific research, collection and analysis of data, determining solutions highlighting individuals' contribution. Continuous assessment of Mini Project at Mid Sem and End Sem will be monitored by the Departmental committee.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
ENGLISH FOR RESEARCH PAPER WRITING
(AUDIT COURSE)

Course Code: GR22D5153 **L/T/P/C :2/0/0/0**

Course Objectives:
1. Understand how to improve their writing skills and level of readability
2. Learn about what to write in each section
3. Understand the skills needed when writing a Title and ensure the good quality of paper at very first-time submission
4. Understand the process of research
5. Write quality research papers

Course Outcomes:
1. give a view of what writing is all about
2. understand Research and its process
3. comprehend the steps and methods involved in research process
4. have learned various skills necessary that are necessary for doing research
5. have learned how to write quality research papers along with other research areas

UNIT I
Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II
Hedging and Critiquing, Paraphrasing and Plagiarism, Sections of a Paper

UNIT III
A**:** Abstracts and writing an Introduction, Review of the Literature, Methods and Results
B: Key skills that are needed when writing a Title, an Abstract, an Introduction, and Review of the Literature,

UNIT IV
A**.** Methods, the Results, Discussion, Conclusions, the Final Check, Clarifying, Who Did What, Highlighting Your Findings
B**.** Key Skills that are needed when writing the Methods, the Results, the Discussion, and the Conclusion

UNIT V
Useful phrases, how to ensure paper is as good as it could possibly be the first- time **s**ubmission

Text book/Reference Books:
1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Ian Wallwork , English for Writing Research Papers, Springer New York Dordrecht

Heidelberg London, 2011

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
DISASTER MANAGEMENT
(AUDIT COURSE)

Course Code: GR22D5154 **L/T/P/C: 2/0/0/0**

Course Objectives:

1. Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. Critically understand the strengths and weaknesses of disaster management approaches,
5. Planning and programming in different countries, particularly their home country or the countries they work in.

Course Outcomes:

1. Capacity to integrate knowledge and to analyze, evaluate and manage the different public health aspects of disaster events at a local and global levels, even when limited information is available.
2. Capacity to describe, analyze and evaluate the environmental, social, cultural, economic, legal and organizational aspects influencing vulnerabilities and capacities to face disasters.
3. Capacity to work theoretically and practically in the processes of disaster management (disaster risk reduction, response, and recovery) and relate their interconnections, particularly in the field of the Public Health aspects of the disasters.
4. Capacity to manage the Public Health aspects of the disasters.
5. Capacity to obtain, analyze, and communicate information on risks, relief needs and lessons learned from earlier disasters in order to formulate strategies for mitigation in future scenarios with the ability to clearly present and discuss their conclusions and the knowledge and arguments behind them

UNIT I

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural And Manmade Disasters: Difference, Nature, TypesAnd Magnitude.

UNIT II

Repercussions of Disasters and Hazards: **Economic Damage**, Loss of Human And Animal Life, Destruction Of Ecosystem. **Natural Disasters**: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts andFamines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III

Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone To Floods And Droughts, Landslides and Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special References To Tsunami; Post-Disaster Diseases And Epidemics

UNIT IV

Disaster Preparedness and Management: Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data

From Meteorological And Other Agencies, Media Reports: Governmental And CommUNITy Preparedness.

UNIT V

Risk Assessment: Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co- Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival. Concept and Strategies of Disaster Mitigation, Emerging Trendsin Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

SUGGESTED READINGS:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal bookCompany
2. Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, NewDelhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., NewDelhi.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
SANSKRIT FOR TECHNICAL KNOWLEDGE
(AUDIT COURSE)

Course Code: GR22D5155 **L/T/P/C: 2/0/0/0**

Course Objectives:

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning
3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects
4. Enhancing the memory power
5. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

Course Outcomes:

1. Understanding basic Sanskrit alphabets and Understand tenses in Sanskrit Language.
2. Enable students to understand roots of Sanskrit language.
3. Students learn engineering fundamentals in Sanskrit.
4. Students can attempt writing sentences in Sanskrit.
5. Ancient Sanskrit literature about science & technology can be understood

UNIT I

Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences

UNIT II

Order, Introduction of roots, Technical information about Sanskrit Literature

UNIT III

Technical concepts of Engineering-Electrical,Mechanical, Architecture,Mathematics and Applications of OCR for Sanskrit and Indian Languages, Tool and Techniques, Survey

UNIT IV

Interactive Sanskrit Teaching Learning Tools: Interactive Sanskrit Learning Tools, Introduction, WhyInteractive Tools for Sanskrit? E-learning, Basics of Multimedia, Web based tools development HTML, Web page etc., Tools and Techniques

UNIT V

Standard for Indian Languages (Unicode) Unicode Typing in Devanagari Scripts, Typing Tools and Software, Text Processing and Preservation Tools, Text Processing, Preservation,Techniques, Text Processing and Preservation, Tools and Techniques, Survey

Reference Books:

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, NewDelhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-VempatiKutumbshastri, Rashtriya Sanskrit Sansthanam, New DelhiPublication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., NewDelhi.
4. Bharti A., R. Sangal, V. Chaitanya, "NL, Complexity Theory and Logic" in Foundations of Software Technology and Theoretical Computer Science, Springer, 1990.
5. Tools developed by Computational Linguistics Group, Department of Sanskrit, University of Delhi, Delhi-110007 available at: http://sanskrit.du.ac.in

6. Basic concept and issues of multimedia:
   http://www.newagepublishers.com/samplechapter/001697.pdf

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
VALUE EDUCATION
(AUDIT COURSE)

Course Code: GR22D5156 **L/T/P/C: 2/0/0/0**

Course Objectives:
1. Understand value of education and self-development
2. Imbibe good values in students
3. Let the should know about the importance of character
4. To understand the significance of human conduct and self-development
5. To enable students to imbibe and internalize the value and Ethical behaviour in personal and professional lives.

Course Outcomes:
1. Knowledge of self-development
2. Learn the importance of Human Values
3. Developing the Professionalism Ethics, Risks, Responsibilities and Life Skills.
4. Student will be able to realize the significance of ethical human conduct and self-development
5. Students will be able to inculcate positive thinking, dignity of labor and religious tolerance.

UNIT I
Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

UNIT II
Importance of cultivation of values, Sense of duty.Devotion, Self-reliance. Confidence, Concentration. Truthfulness,Cleanliness. Honesty, Humanity. Power of faith, National UNITy. Patriotism. Love for nature, Discipline

UNIT III
Personality and Behaviour Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

UNIT IV
Character and Competence –Holy books vs Blind faith. Self-management and Good health.Science ofreincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind,Self-control. Honesty, Studying effectively

UNIT V
Introduction to Professional Ethics: Basic Concepts, Governing Ethics, Personal & Professional Ethics, Ethical Dilemmas, Life Skills, Emotional Intelligence, Thoughts of Ethics, Value Education, Dimensions of Ethics, Profession and professionalism, Professional Associations, Professional Risks, Professional Accountabilities, Professional Success, Ethics and Profession.

Reference Books:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi
2. Jagdish Chand, “Value Education”
3. N. Venkataiah, “ Value Education”, APH Publishing, 1998 - Education

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

INDIAN CONSTITUTION
(AUDIT COURSE)

Course Code: GR22D5157 **L/T/P/C :2/0/0/0**

Course Objectives:
1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals 'constitutional
3. Role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
4. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.
5. To understand the role and functioning of Election Commission of India.

Course Outcomes:
1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of1956.
5. Discuss the significance of Election Commission of India.

UNIT I
History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working)

UNIT II
Philosophy of the Indian Constitution: Preamble Salient Features

UNIT III
Contours of Constitutional Rights &Duties: FundamentalRights, Right toEquality, Right toFreedom, Right againstExploitation, Right to Freedom ofReligion, Cultural and EducationalRights, Right to ConstitutionalRemedies, Directive Principles of StatePolicy, FundamentalDuties.

UNIT IV
Organs ofGovernance and composition of judiciary: Parliament- Composition, Qualifications andDisqualifications, Powers andFunctions, Executive, President, Governor, Council ofMinisters, composition of judiciary, Appointment and Transfer of Judges,Qualifications, Powers andFunctions

UNIT V

LocalAdministration and Election Commission: District's Administration head: Role andImportance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of MunicipalCorporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position androle. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointedofficials, Importance of grass rootdemocracy.**ElectionCommission:** Election Commission: Role andFunctioning, Chief Election Commissioner and ElectionCommissioners, State Election Commission: Role andFunctioning

Text Books/References

1. The Constitution of India, 1950 (Bare Act), GovernmentPublication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition,2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis,2015.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
PEDAGOGY STUDIES
(AUDIT COURSE)

Course Code: GR22D5158 **L/T/P/C: 2/0/0/0**

Course Objectives:

1. Review existing evidence on the review topic to inform Programme design and policy making
2. Undertaken by the DFID, other agencies and researchers.
3. Identify critical evidence gaps to guide the development.
4. Establishing coordination among people in order to execute pedagogy methods.
5. To study pedagogy as a separate discipline.

Course Outcomes:

1. What pedagogical practices are being used by teachers in formal classrooms in developing countries
2. What pedagogical practices are being used by teachers in informal classrooms in developing countries?
3. Synergy from the work force.
4. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
5. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

UNIT I

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

UNIT II

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT III

Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT IV

Professional development: alignment with classroom practices and follow- up support, Peer support, Support from the head teacher and the community, Curriculum and assessment, Barriers to learning: limited resources and large class sizes

UNIT V

Research gaps and future directions: Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

Text Books/References

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3):361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London:DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3):272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston:Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read'campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
STRESS MANAGEMENT BY YOGA
(AUDIT COURSE)

Course Code: R22D5159 **L/T/P/C: 2/0/0/0**

Course Objective:
1. To achieve overall health of body and mind.
2. To overcome stress.
3. To lower blood pressure and improve heart health.
4. Relaxation and Sleeping aid and to become non-violent and truthfulness.
5. To increase the levels of happiness and to eliminate all types of body pains.

Course Outcomes:
1. Develop healthy mind in a healthy body thus improving social health also improve efficiently.
2. Develop body awareness. Learn how to use their bodies in a healthy way. Perform well in sports and academics.
3. Will balance, flexibility, and stamina, strengthen muscles and connective tissues enabling good posture.
4. Manage stress through breathing, awareness, meditation and healthy movement.
5. Build concentration, confidence and positive self-image

UNIT I
Definitions of Eight parts of yoga. (Ashtanga)
Ashtanga, the eight limbs of yoga, is Patanjali's classification of classical yoga, as set out in his Yoga Sutras. He defined the eight limbs as yama (abstinences), niyama (observances), asana (postures), pranayama (breathing), pratyahara (withdrawal), dharana (concentration), dhyana (meditation) and Samadhi (absorption).

UNIT II
Orientation to Patanjala Yoga sutra:
Introduction to Yoga sutra - Nature of Yoga science, Definition of yoga, the nature of seer in pure and modified state, Vrittis - Nature, classification, definition, method to control of chittavrittis. Samprajnata Samadhi and its classification, Iswarapranidhana - a means to attain Samadhi, definition and quality of Iswara. Astanga yoga-Vama, Niyama, Asana, Pranayama, Ratyahara-Bahiranga Yoga, Dharana, Dhyana, Samadhi-Antaranga Yoga, Powers Introduction.

UNIT III
Orientation of Hath yoga pradipika :
Hath yoga - Introduction, relationship of Hath yoga and Raja yoga, greatness of Hath yoga, Hath yogi parampara, importance of Hath and its secrecy, place of Hath yoga Practice, Destructives and constructive of yoga, Yama and Niyama, Asana, methods of Hath yoga Practice, Mitahara, Pathya and Apathya. Rules in food taking, Hath yoga achievements. Paranayama - Benefits of Pranayama, Nadishuddi and Pranayama. Duration and time for pranayama practice, Gradation of Pranayama, Sweat and Pranayama, Food during pranayama practice, Yukta and Ayukta pranayama, Nadishuddi, Satkriya-Neti, Dhouti, Basti, Nauli, Trataka, Kapalbhati, Gajakarani, Importance of Pranayama practice. Symtoms of Nadishuddhi, Manonnani, Varieties of Kumbhaka-Methods of practice, Classification of

their benefits, Hathayogasiddhilakshanam. Kundalini as base for all yoga, Results of Kundalini prabyodha, Synonyms for Susumna, Mudras Bandhas-classification, benefits and methods of practice, Nadanusandhana.

UNIT IV

Yam and Niyam. Do`s and Don'ts in life. Ahinsa, satya, astheya, bramhacharya & aparigraha Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

UNIT V

Asan and Pranayam - Various yoga poses and their benefits for mind & body. Regularization of breathing techniques and its effects-Types of pranayam

Suggested reading

1. 'Yogic Asanas for Group Training - Part-I" : Janardan Swami YogabhyasiMandal,Nagpur
2. "Rajayoga or onquering the Internal Nature" by SwamiVivekananda, AdvaitaAshrama(Publication Department),Kolkata
3. Rajayoga - Swami Vivekananda - Ramakrishna Ashrama Publications.
4. HathayogaPradipika of Swatmarama - Kaivalyadhama, Lonavala
5. The Science of Yoga - Taimini - Theosophical Publishing House, Adyar, Madras.
6. Yogasutras of Patanjali - HariharanandaAranya, University of Calcutta Press, Calcutta.
7. Patanjal Yoga PradeepaOmananda Tirtha- Geeta Press, Gorakhpur.
8. Gherandasamhita - Bihar School of Yoga, Munger, Bihar.
9. Shivayogadipika - Sadashivabrahmendra, Ananda Ashramagranthavali, Choukhamba Press
10. Yoga Darshan : Swami Niranjanananda-Sri PanchadashanamParamahamsaAlakh Bara, Deoghar.
11. Four chapters on Freedom (commentary on the Yoga sutras of Patanjali), Swami Satyananda (1983), Bihar School of Yoga, Munger.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(AUDIT COURSE)

Course Code: GR22D5160 **L/T/P/C: 2/0/0/0**

Course Objectives:

1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students
4. To differentiate three types of happiness (Sukham)
5. To describe the character traits of a spiritual devotee

Course Outcomes:

1. Study of Shrimad- Bhagwad-Gita wiil help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neethishatakam will help in developing versatile personality of students
4. To develop self-developing attitude towards work without self-aggrandizement and to develop suffering free meditative mind
5. To develop tranquil attitude in all favorable and unfavorable situations and to develop high spiritual intelligence

UNIT I

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT II

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT III

Approach to day to day work and duties.

- Shrimad Bhagwad Geeta: Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

UNIT IV

Statements of basic knowledge.

- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:

UNIT V

- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

TEXT BOOKS/ REFERENCES:

1. "Srimad Bhagavad Gita" by Swami SwarupanandaAdvaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

II YEAR
I SEMESTER

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

CPLD AND FPGA ARCHITECURES
(PROFESSIONAL ELECTIVE V)

Course Code: GR22D5091 **L/T/P/C: 3/0/0/3**
II Year I Semester

Course Objectives:
1. To understand the concept of Programmable Logic Device architectures and technologies.
2. Underlying FPGA architectures and technologies in detail.
3. To understand the difference between CPLDs and FPGAs.
4. To provide knowledge about SRAM Programmable FPGA Device architecture.
5. To comprehend knowledge about Anti-Fuse Programmable FPGA Device architecture.

Course Outcomes:
1.To know the concept of program able architectures.
2.Perceiving CPLD and FPGA technologies.
3.Study and compare the different architectures of CPLDs and FPGAs.
4.An ability to know the SRAM Technology based FPGAs.
5.An ability to know the Anti-Fuse Technology based FPGAs

UNIT I
INTRODUCTION TO PROGRAMMABLE LOGIC DEVICES
Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT II
FIELD PROGRAMMABLE GATE ARRAYS Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT III
SRAM PROGRAMMABLE FPGA'S Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT IV
ANTI-FUSE PROGRAMMED FPGA'S Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT V
DESIGN APPLICATIONS General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

Reference Books:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
VLSI SIGNAL PROCESSING
(PROFESSIONAL ELECTIVE V)

Course Code: GR22D5092 **L/T/P/C: 3/0/0/3**
II Year I Semester

Course Objectives:
1. To train the students on various DSP architectures useful to VLSI Design
2. To learn the students about various algorithms related to folding and unfolding.
3. To give the clear idea about 2D systolic array design for space representation contains delays
4. To give the knowledge of various algorithms useful to convolution operations, system responses
5. To train the students about signal processors for wireless applications

Course Outcomes:
1. Ability to modify the existing or new DSP architectures suitable for VLSI.
2. Understand the concepts of folding and unfolding algorithms and applications.
3. Understand 2D systolic array design for space representations.
4. Ability to implement fast convolution algorithms.
5. Low power design aspects of processors for signal processing and wireless applications.

UNIT I
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP

Algorithms Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

UNIT II
Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems
Unfolding: Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

UNIT III
Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT IV
Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection.

UNIT V
Low Power Design: Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications,

Processors for Multimedia Signal Processing

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parthi, WileyInter Science, 1998.
2. VLSI and Modern Signal processing – Kung S. Y, H. J. While House, T. Kailath, Prentice Hall,1985.

REFERENCE BOOKS:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, Prentice Hall, 1994.
2.VLSI Digital Signal Processing – Medisetti V. K, IEEE Press (NY), 1995

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
CMOS MIXED SIGNAL CIRCUIT DESIGN
(PROFESSIONAL ELECTIVE V)

Course Code: GR22D5093 **L/T/P/C: 3/0/0/3**
II Year I Semester

Course Objectives:
1. This course provides the concepts of switched capacitor circuits used in mixed signal circuit design.
2. To know mixed signal circuits like DAC,ADC,PLL etc.,
3. To acquire knowledge on design different architectures in mixed signal mode.
4. To gain knowledge on noise shaping modulators and higher order modulators.
5. It deals with the design and analysis of Biquad Filters.

Course outcomes
1. Analyze and design of switched capacitor circuits used in mixed signal circuit design
2. Design noise shaping converters given a set of requirements such as bandwidth, clock speed and signal-to-noise ratio
3. design an integrated mixed signal circuit in CMOS using modern design tools
4. Demonstrate in-depth knowledge in PLL and Data Converters (DAC and ADC)
5. Analyze complex engineering problems critically for conducting research in data converters

UNIT I
Switched Capacitor Circuits
Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT II
Phased Lock Loop (PLL)
Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT III
Data Converter Fundamentals
DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT IV
Nyquist Rate A/D Converters
Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT V

Oversampling Converters

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizes, Delta sigma D/A

Text Books:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

Reference Books:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Inderscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Inderscience, 2009.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

COST MANAGEMENT OF ENGINEERING PROJECTS
(OPEN ELECTIVE)

Course Code: GR22D5147 **L/T/P/C: 3 /0 /0 /3**
II Year I Semester

Course Objectives:
1. To provide the student with a clear understanding of the strategic cost management process.
2. To describe the various stages of project execution.
3. To prepare the project schedule by bar charts and network diagrams.
4. To conduct breakeven and cost-volume-profit analysis.
5. To make students understand various budgets and quantitative techniques used for cost management.

Course Outcomes:
1. Explain the various cost concepts used in decision making.
2. Identify and demonstrate various stages of project execution.
3. Prepare the project schedule by bar charts and network diagrams.
4. Differentiate absorption costing and marginal costing, also conduct breakeven and cost-volume-profit analysis.
5. Prepare various budgets and quantitative techniques used for cost management.

UNIT I
Introduction and Overview of the Strategic Cost Management Process, Cost concepts in decision-making; relevant cost, Differential cost, Incremental cost, Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

UNIT II
Project: Meaning, Different types, why to manage, cost overruns centres, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and non- technical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process.

UNIT III
Cost Behaviour and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision- making problems. Standard Costing and Variance Analysis. Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints. Activity- Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis.

UNIT IV
Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets.

Measurement of Divisional profitability pricing decisions including transfer pricing.

UNIT V

Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

TEXT/REFERENCE BOOKS :

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi.
2. Charles T. Horngren and George Foster, Advanced Management Accounting.
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting.
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher.
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co.Ltd

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
INDUSTRIAL SAFETY
(OPEN ELECTIVE)

Course Code: GR22D5148 **L/T/P/C: 3/0/0/3**
II Year I Semester

Course Objectives:
1. To understand the importance of maintaining a safe workplace.
2. To maintain safety standards in compliance with regulatory requirements and within engineering limits understand personal safety and industrial safety.
3. To create a job safety analysis (JSA) for a given work project.
4. To follow safety recordkeeping and management, and the role of the safety manager.
5. To utilize personal proactive equipment.

Course Outcomes:
1. Understanding of Safety principles.
2. Analyze different types of exposure and biological effects, exposure guidelines and basic workplace monitoring Ability to do Hazard analysis.
3. Demonstrate an understanding of workplace injury prevention, risk management, and incident investigations.
4. Understand the acute and chronic health effects of exposures to chemical, physical and biological agents in the workplace.
5. Demonstrate knowledge of the types of hazards, planning, organization and training needed to work safely with hazardous materials.

UNIT I
Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT II
Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III
Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wickfeed lubrication vi. Sidefeed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT IV

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT V

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: i. Machine tools, ii. Pumps, iii. Air compressors,iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance.

TEXT/REFERENCE BOOKS:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da InformationServices.
2. Maintenance Engineering, H. P. Garg, S. Chand andCompany.
3. Pump-hydraulic Compressors, Audels, McgrewHillPublication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman &HallLondon.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

OPERATIONS RESEARCH
(OPEN ELECTIVE)

Course Code: GR22D5149 **L/T/P/C:3/0/0/3**
II Year I Semester

Course Objectives:
1. To define and formulate linear and Non-linear programming problems and appreciate their limitations arising from a wide range of applications.
2. To perform sensitivity analysis to determine the direction and magnitude of change of a model's optimal solution as the data change.
3. To distinguish various inventory models and develop proper inventory policies.
4. To solve the scheduling and sequencing models.
5. To understand how to model and solve problems using dynamic programming, Game Theory.

Course Outcomes:
1. The student will able to carry out sensitivity analysis.
2. The student will solve network models like the shortest path, minimum spanning tree, and maximum flow problems.
3. The student will able to distinguish various inventory models and develop proper inventory policies.
4. The student will also propose the best strategy using decision making methods under uncertainty and game theory.

UNIT I
Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex techniques, Sensitivity Analysis, Inventory Control Models.

UNIT II
Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming.

UNIT III
Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem -CPM/PERT.

UNIT IV
Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

UNIT V
Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation

TEXT/REFERENCE BOOKS:

1. H.A. Taha, Operations Research, An Introduction, PHI,2008
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi,1982.
3. J.C. Pant, Introduction to Optimization: Operations Research, Jain Brothers, Delhi,2008
4. Hitler Libermann Operations Research: McGraw Hill Pub.2009
5. Pannerselvam, Operations Research: Prentice Hall of India2010
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India2010

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY

ARTIFICIAL NEURAL NETWORKS AND FUZZY SYSTEMS
(OPEN ELECTIVE)

Course Code: GR22D5150 **L/T/P/C: 3/0/0/3**
II Year I Semester

Course Objectives:
1. To cater the knowledge of Neural Networks and Fuzzy Logic Control and use these for controlling real time systems.
2. To know about feedback networks.
3. To learn about the concept of fuzziness involved in various systems
4. To understand the concept of adequate knowledge about fuzzy set theory.
5. To learn about comprehensive knowledge of fuzzy logic control and adaptive fuzzy logic and to design the fuzzy control using genetic algorithm

Course Outcomes:
1. To Expose the students to the concepts of feed forward neural networks
2. To provide adequate knowledge about feedback networks.
3. To teach about the concept of fuzziness involved in various systems.
4. To provide adequate knowledge about fuzzy set theory.
5. To provide comprehensive knowledge of fuzzy logic control and adaptive fuzzy logic and to design the fuzzy control using genetic algorithm.

UNIT I

Introduction To Neural Networks: Introduction, Humans and Computers, Organization of the Brain, Biological Neuron, Biological and Artificial Neuron Models, Hodgkin-Huxley Neuron Model, Integrate-and-Fire Neuron Model, Spiking Neuron Model, Characteristics of ANN, McCulloch-Pitts Model, Historical Developments, Potential Applications of ANN.

UNIT II

Essentials Of Artificial Neural Networks: Artificial Neuron Model, Operations of Artificial Neuron, Types of Neuron Activation Function, ANN Architectures, Classification Taxonomy of ANN – Connectivity, Neural Dynamics (Activation and Synaptic), Learning Strategy (Supervised, Unsupervised, Reinforcement), Learning Rules, Types of Application.

Feed Forward Neural Networks

Introduction, Perceptron Models: Discrete, Continuous and Multi-Category, Training Algorithms: Discrete and Continuous Perceptron Networks, Perceptron Convergence theorem, Limitations of the Perceptron Model, Applications

UNIT III

Multilayer Feed Forward Neural Networks

Credit Assignment Problem, Generalized Delta Rule, Derivation of Backpropagation (BP) Training, Summary of Backpropagation Algorithm, Kolmogorov Theorem, Learning Difficulties and Improvements.

Associative Memories

Paradigms of Associative Memory, Pattern Mathematics, Hebbian Learning, General Concepts of Associative Memory (Associative Matrix, Association Rules, Hamming Distance, The Linear Associator, Matrix Memories, Content Addressable Memory), Bidirectional

Associative Memory (BAM) Architecture, BAM Training Algorithms: Storage and Recall Algorithm, BAM Energy Function, Proof of BAM StabilityTheorem. Architecture of Hopfield Network: Discrete and Continuous versions, Storage and Recall
Algorithm, Stability Analysis, Capacity of the Hopfield Network.

UNIT IV

Self-Organizing Maps (Som) And Adaptive Resonance Theory (Art)

Introduction, Competitive Learning, Vector Quantization, Self-Organized Learning Networks, Kohonen Networks, Training Algorithms, Linear Vector Quantization, Stability- Plasticity Dilemma, Feed forward competition, Feedback Competition, Instar, Outstar, ART1, ART2, Applications. Classical& Fuzzy Sets Introduction to classical sets - properties, Operations and relations; Fuzzy sets, Membership, Uncertainty, Operations, properties, fuzzy relations, cardinalities, membershipfunctions.

UNIT V

Fuzzy Logic System Components

Fuzzification, Membership value assignment, development of rule base and decision making system, Defuzzification to crisp sets, Defuzzification methods. Applications

Neural network applications: Process identification, Function Approximation, control and Process Monitoring, fault diagnosis and load forecasting.

Fuzzy logic applications: Fuzzy logic control and Fuzzy classification

TEXT/REFERENCE BOOKS:

1. Neural Networks, Fuzzy logic, Genetic algorithms: synthesis and applications by Rajasekharan and Rai – PHIPublication.
2. Introduction to Artificial Neural Systems - Jacek M. Zuarda, Jaico Publishing House,1997.
3. Neural and Fuzzy Systems: Foundation, Architectures and Applications, - N. YadaiahandS. BapiRaju, PearsonEducation
4. Neural Networks – James A Freeman and Davis Skapura, Pearson,2002.
5. Neural Networks – Simon Hykins , Pearson Education
6. Neural Engineering by C.Eliasmith and CH.Anderson,PHI
7. Neural Networks and Fuzzy Logic System by Bork Kosko, PHIPublications.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
CYBER SECURITY
(OPEN ELECTIVE)

Course Code: GR22D5151 **L/T/P/C: 3/0/0/3**
II Year I Semester

Course Objectives:
1. To understand Cyber security challenges and their threats.
2. To understand Cyber attacks and their vulnerabilities.
3. To understand ethical hacking concepts and social engineering targets.
4. To understand cyber forensic investigation process
5. To recognize cyber laws and ethics

Course Outcomes:
1. Understand importance and challenges of Cyber security
2. Investigate cybercrime and collect evidences
3. Identify security risks and take preventive steps
4. Able to use knowledge of forensic tools and software
5. Knowledge about Indian IT act and International law

UNIT I
Introduction to Cyber Security: Introduction to Cyber Security, Importance and challenges in Cyber Security, Cyberspace, Cyber threats, Cyber warfare, CIA Triad, Cyber Terrorism, Cyber Security of Critical Infrastructure, Cyber security - Organizational Implications.

UNIT II
Hackers and Cyber Crimes: Types of Hackers, Hackers and Crackers, Cyber-Attacks and Vulnerabilities, Malware threats, Sniffing, Gaining Access, Escalating Privileges, Executing Applications, Hiding Files, Covering Tracks, Worms, Trojans, Viruses, Backdoors.

UNIT III
Ethical Hacking and Social Engineering: Ethical Hacking Concepts and Scopes, Threats and Attack Vectors, Information Assurance, Threat Modelling, Enterprise Information Security Architecture, Vulnerability Assessment and Penetration Testing, Types of Social Engineering, Insider Attack, Preventing Insider Threats, Social Engineering Targets and Defence Strategies.

UNIT IV
Cyber Forensics and Auditing: Introduction to Cyber Forensics, Computer Equipment and associated storage media, Role of forensics Investigator, Forensics Investigation Process, and Collecting Network based Evidence, Writing Computer Forensics Reports, Auditing, Plan an audit against a set of audit criteria, Information Security Management System Management. Introduction to ISO 27001:2013

UNIT V
Cyber Ethics and Laws: Introduction to Cyber Laws, E-Commerce and E-Governance, Certifying Authority and Controller, Offences under IT Act, Computer Offences and its penalty under IT Act 2000, Intellectual Property Rights in Cyberspace.

TEXT/REFERENCE BOOKS:

1. Donaldson, S., Siegel, S., Williams, C.K., Aslam, A., Enterprise Cybersecurity -How to Build a SuccessfulCyberdefense Program Against Advanced Threats, A-press .
2. Nina Godbole, SumitBelapure, Cyber Security, Willey
3. Hacking the Hacker, Roger Grimes, Wiley
4. Cyber Law By Bare Act, Govt Of india, It Act 2000.

GOKARAJU RANGARAJU INSTITUTE OF ENGINEERING AND TECHNOLOGY
INTERNET OF THINGS ARCHITECTURE AND DESIGN PRINCIPLES
(OPEN ELECTIVE)

Course Code: GR22D5152 **L/T/P/C: 3/0/0/3**
II Year I Semester

Course Objectives:
1. To assess the vision and introduction of IoT.
2. To Understand Networking & Communication aspects of IOT.
3. To Explore the Application areas of IOT and to analyze the current needs
4. To Understand State of the Art - IoT Architecture.
5. To classify Real World IoT Design Constraints, Industrial Automation in IoT.

Course Outcomes:
1. Understand the concepts of Internet of Things
2. Analyze basic protocols in wireless sensor network
3. Design IoT applications in different domain and be able to analyze their performance
4. Understand the Hardware concepts of Internet of Things
5. Implement basic IoT applications through python.

UNIT 1
Introduction to IoT : Defining IoT, Characteristics of IoT, Physical design of IoT, Logical design of IoT, Functional blocks of IoT, Communication models & APIs**IoT & M2M** Machine to Machine, Difference between IoT and M2M, Software define Network.

UNIT II
Network & Communication aspects Connectivity terminologies-IOT Node, LAN,WAN, Gateway, IOT Stack vs. Web Stack, IOT Identification and Data Protocols-IPV4,IPV6,HTTP,MQTT,COAP

UNIT III
IOT Applications Smart Homes-Smart Home Origin, Technologies, Implementation, Smart Grids-Characteristics, Benefits, Architecture, Components, Smart Cities-Characteristics, Frameworks, Challenges, Industrial IOT- Requirements, Design Considerations, Applications

UNIT IV
Hardware Platforms Programming with Arduino-Features of Arduino, Components of Arduino Board, Arduino IDE, Program Elements, Raspberry

UNIT V
Developing IoTs Introduction to Python, Introduction to different IoT tools, developing applications through IoT tools, developing sensor based application through embedded system platform, Implementing IoT concepts with python.

Text Books:
1. Vijay Madisetti, Arshdeep Bahga, “Internet of Things: A Hands-On Approach”
2. Internet of Things, Jeeva Jose, Khanna Publishing, 2018
3. Waltenegus Dargie, Christian Poellabauer, "Fundamentals of Wireless Sensor Networks: Theory and Practice".

Reference Books:

1. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, Stamatis Karnouskos, David Boyle, "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", 1 st Edition, Academic Press, 2014. (ISBN-13: 978-0124076846).
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything",1st st Edition, Apress Publications, 2013. (ISBN-13: 978- 1430257.
3. Internet of Things Challenges, Advances and Applications by Quas F.Hassan, Atta Ur Rehaman Khan, and Sajiad A. Madani