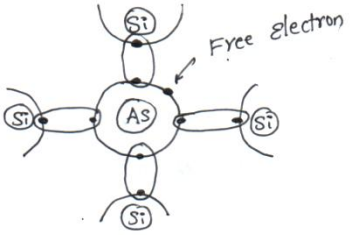
Unit-I

Semiconductors and pn Junction Diode

1. **Explain N-type and P-type semiconductors.**

Ans: n- type semiconductor

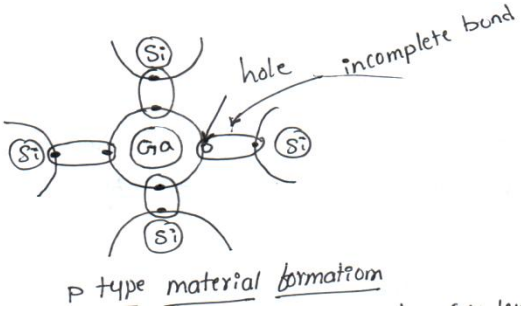
- When a small amount of pentavalent impurity is added to a pure semiconductor, it is called n-type semiconductor.
- The pentavalent impurity is also called donor impurity has five valence electrons.
- Examples: *Phosphorous, Arsenic, Antimony, Bismuth*.
- Consider the formation of n type material by adding Arsenic(As) into Silicon(Si).



- The As atom has five valence electrons. An As atom fits in the silicon crystal in such a way that its four valence electrons from covalent bonds with four adjacent Si atoms.
- The fifth electron has no chance of forming a covalent bond. It enters the conduction band as a free electron.
- One donor impurity atom donates one free electron in n- type material. The free electrons are majority charge carriers.

p- type semiconductor

- When a small amount of trivalent impurity is added to a pure semiconductor, it is called p-type semiconductor.
- The trivalent impurity is also called acceptor impurity has three valence electrons.
- Examples: *Boron, Aluminium, Gallium, Indium*.
- Consider the formation of p- type material by adding Gallium(Ga) into Silicon(Si).



- The Ga atom has three valence electrons, the fourth covalent bond in the valence shell is incomplete. The resulting vacancy is called a hole.
- This means that each Ga atom added into Si atom gives one hole.
- One acceptor impurity creates one hole in a p- type material. The holes are majority charge carriers.

2. Write short notes on Diffusion and Drift current.

Ans: Diffusion current: The flow of charge carriers from a high density region to low density region constitute diffusion current. This flow occurs until the distribution of charges becomes uniform, in both regions.

The diffusion current density due to hole is given by,

$$J_p = -qD_p \frac{dp}{dx}$$

The diffusion current density due to electron is given by

$$J_n = qD_n \frac{dn}{dx}$$

Where q = charge of electron

D_p = diffusion constant for hole m^2/sec

D_n = diffusion constant for electron m^2/sec

$\frac{dp}{dx}$ = concentration of gradient for holes

$\frac{dn}{dx}$ = concentration of gradient for electrons.

Drift current : Whenever voltage is applied to the pn junction, there exist a flow of current because of applied voltage and this current is known as drift current.

The drift current density due to hole is given by, $J_p = qp\mu_p E$

The drift current density due to free electron is given by, $J_n = qn\mu_n E$

Total drift current density $J_{total} = qp\mu_p E + qn\mu_n E$

Where p = no.of holes/cm^3

n = no.of free electrons /cm^3

μ_p = mobility of hole

μ_n = mobility of electron

E = electric field intensity

3.State law of mass action and the Einstein's relationship for semiconductor.

Ans: Law of mass action: It states that the product of concentrations of electrons and holes is always constant, at a fixed temperature.

$$np = n_i^2$$

Where n = concentration of electrons

p = concentration of holes

n_i = intrinsic concentration

For n-type material , n = n_n while p = p_n hence law can be stated as $n_n p_n = n_i^2$

For p-type material , n = n_p while p = p_p hence law can be stated as $n_p p_p = n_i^2$

Einstein's relationship: It states that, at a fixed temperature, the ratio of diffusion constant to the mobility contant.

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = KT = V_T$$

Where K= Boltzmann's constant = 8.62×10^{-5} ev/^{o}k

T = temperature in ^{o}k

KT= V_T = voltage equivalent of temperature.

At room temperature $V_T = 0.02586V$ or $V_T = \frac{T}{11600}$

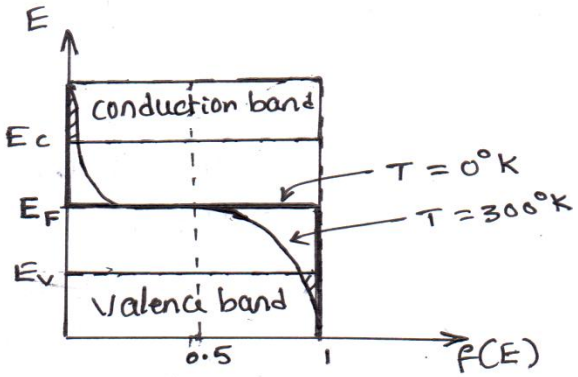
4. Explain the Fermi's level in intrinsic semiconductor.

(or)

Show that the Fermi energy level lies in the center of forbidden energy band for an intrinsic semiconductor.

Ans: In intrinsic semiconductor the probability of finding an electron in the conduction band is zero and probability of finding a hole in the valence band is zero at T=0°k. At temperature increases, equal number of electrons and holes get generated. In such a case the Fermi level E_F is given by

$$E_F = \frac{E_C + E_V}{2}$$



Energy band diagram

Proof:

In a pure semiconductor the number of holes and electrons are equal.

That is $n = p = n_i$

$$N_C e^{-(E_C - E_F)/kT} = N_V e^{-(E_F - E_V)/kT}$$

$$\frac{N_C}{N_V} = \frac{e^{-(E_F - E_V)/kT}}{e^{-(E_C - E_F)/kT}} = e^{(-E_F + E_V + E_C - E_F)/kT}$$

$$\frac{N_C}{N_V} = e^{(E_C + E_V - 2E_F)/kT}$$

Taking logarithm on both sides

$$\ln\left(\frac{N_C}{N_V}\right) = \frac{E_C + E_V - 2E_F}{kT}$$

$$E_C + E_V - 2E_F = kT \ln \frac{N_C}{N_V}$$

$$2E_F = E_C + E_V - kT \ln \frac{N_C}{N_V}$$

$$E_F = \frac{E_C + E_V}{2} - \frac{kT}{2} \ln \frac{N_C}{N_V}$$

If $N_C = N_V$, $E_C + E_F - 2E_F = 0$

and $2E_F = E_C + E_V$

$$E_F = \frac{E_C + E_V}{2}$$

5. Explain about Fermi level in extrinsic semiconductor.

Ans: Fermi level in n type semiconductor:

- The donor impurity added is just below the conduction band. This donor level is indicated as E_D .
- As this distance is very small, even at room temperature almost all the extra electrons from the donor impurity atoms jump into the conduction band.
- The probability of occupying the energy level by the electrons, towards the conduction band is more.
- So in n- type material, the Fermi level E_F gets shifted towards the conduction band. But it is below the donor energy level.

$$n \simeq N_D$$

$$n = N_C e^{(E_F - E_C)/kT}$$

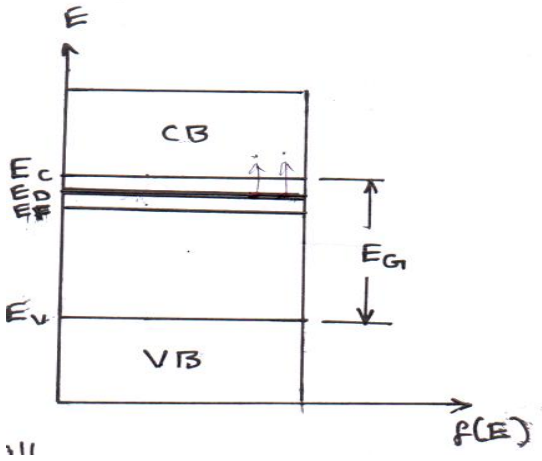
$$N_D = N_C e^{(E_F - E_C)kT}$$

$$\frac{N_D}{N_C} = e^{(E_F - E_C)/kT}$$

$$\ln \frac{N_D}{N_C} = \frac{E_F - E_C}{kT}$$

$$-kT \ln \frac{N_C}{N_D} = E_F - E_C$$

$$E_F = E_C - kT \ln \left(\frac{N_C}{N_D} \right)$$



Fermi level in P type semiconductor:

- In p-type material, acceptor impurity is added just above the valence band.
- Due to this, large number of holes gets generated in the valence band.
- At room temperature, the electrons from valence band jump to acceptor energy level, leaving behind the holes in valence band.
- This shifts the Fermi level E_F towards the valence band. It lies above the acceptor energy level.

$$p \simeq N_A$$

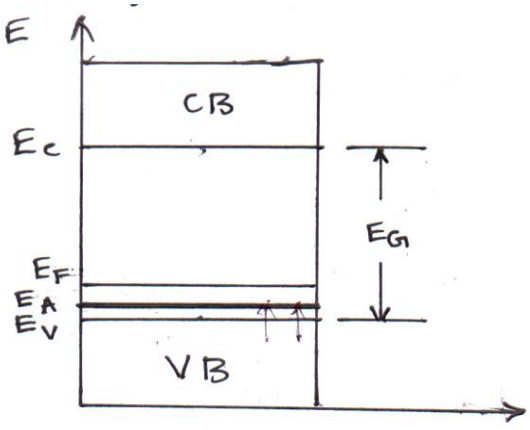
$$\text{Hence} \quad N_A = N_V e^{-(E_F - E_V)/kT}$$

$$\frac{N_A}{N_V} = e^{-(E_F - E_V)/kT}$$

$$\ln \frac{N_A}{N_V} = -\frac{(E_F - E_V)}{kT}$$

$$kT \ln \frac{N_A}{N_V} = -(E_F - E_V)$$

$$\Rightarrow \quad E_F = E_V + kT \ln \frac{N_V}{N_A}$$



6.Explain the formation of depletion region in an open circuited p-n junction with neat sketches. (or)

With the help of necessary sketches, explain the potential distribution in an open circuited p-n junction.

Ans:

- When two extrinsic semiconductors, one p-type and another n-type are joined, a p-n junction is formed.
- The holes from p-side and electrons from n-side which form majority carriers in their respective sections are diffused in either direction.
- At this stage p-side will loose its holes and hence a negative field exists towards left side of the junction.
- Similarly, n-side will loose its electrons and hence a positive field exists towards right side of the junction.
- The net result is that an electrical field exists across the junction. This field is known as potential barrier or contact potential.
- Potential barrier will be limited because the negative field on p- side and positive of n-side prevents further displacement of electrons and holes on either side respectively.
- The charge distribution is shown in figure.

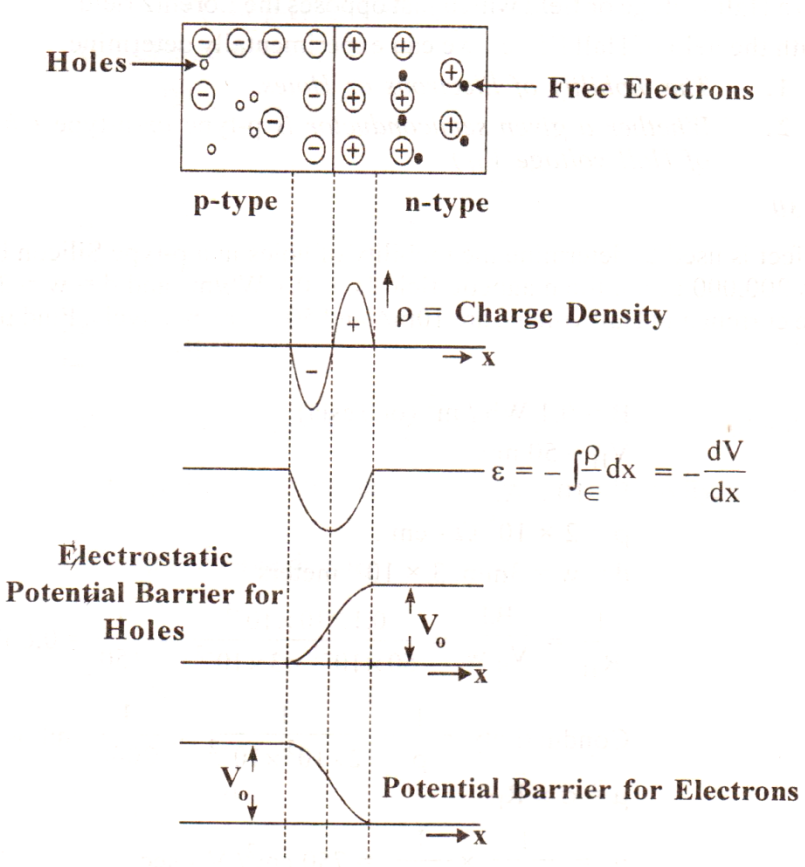


Fig: Potential Distribution in p-n junction Diode

- The concentration of charge decrease as we move away from the junction. Because at the junction, holes and electrons are combined and become neutral.
- The junction is depleted of mobile charges. The region is called space charge region and its thickness is about few microns.
- The electric field intensity, which is the integral of density function ρ is shown in the figure.
- Contact potential as shown in the figure will be of the order of few tenths of volts. Its value of germanium is 0.3V and silicon is 0.7V.

7. Draw the energy band diagram of p-n junction under open circuit conditions and explain. (or)
Derive expression for pn junction diode barrier potential.
(or)
Explain how the built-in potential difference exists at pn junction without the application of an external voltage across it.

Ans:

- It is known that the Fermi level in n-type material lies just below the conduction band while in p-type material, it lies just above the valence band.
- When p-n junction is formed, the diffusion starts. The changes get adjusted so as to equalize the Fermi level in the two parts of p-n junction.
- This is similar to adjustment of water levels in two tanks of unequal level, when connected each other.
- The changes flow from p to n and n to p side till, the Fermi level on two sides get lined up.
- In n-type semi conductor , E_F is close to conduction band E_{cn} and it is close to valence band edge E_{VP} on p-side.
- So the conduction band edge of n-type semiconductor can't be at the same level as that of p-type semiconductor.
- Hence, as shown, the energy band diagram for p-n junction is where a shift in energy levels E_0 is indicated.

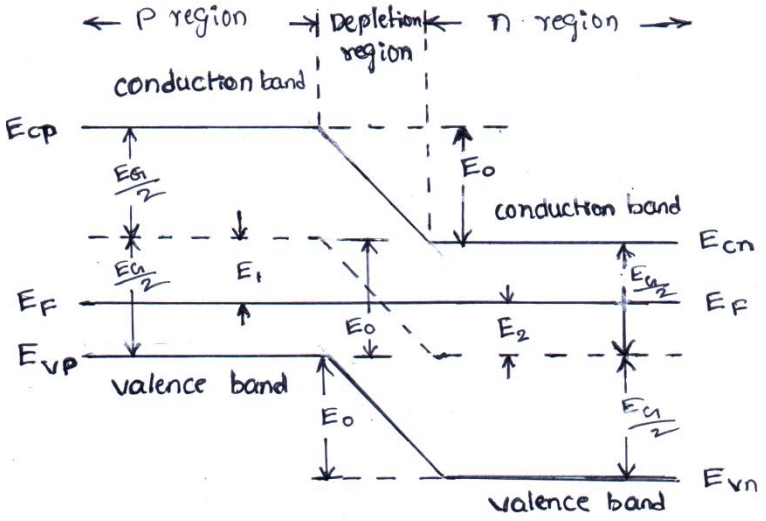


Fig:Energy Band Diagram for p-n Junction under open-circuit Conditions

we know that, for n-type, $E_F = E_{Cn} - kT \ln\left[\frac{N_C}{N_D}\right]$

$$E_{Cn} - E_F = kT \ln\left[\frac{N_C}{N_D}\right] \cdots\cdots\cdots\cdots\cdots\cdots (1)$$

for p-type, $E_F = E_{Vp} + kT \ln\left[\frac{N_V}{N_A}\right]$

$$E_F - E_{Vp} = kT \ln\left[\frac{N_V}{N_A}\right] \cdots\cdots\cdots\cdots\cdots\cdots (2)$$

Since, $n = p = n_i \; and \; np = n_i^2$

In N-type, $n_n \cong N_D$

$$n_n p_n \cong n_i^2$$

$$p_n = \frac{n_i^2}{N_D} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (3)$$

In P-type $p_p \cong N_A$

$$n_p p_p \cong n_i^2$$

$$n_p = \frac{n_i^2}{N_A} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (4)$$

From the energy band diagram

$$E_{Cn} - E_F = \frac{E_G}{2} - E_2 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (5)$$

$$E_F - E_{Vp} = \frac{E_G}{2} - E_1 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (6)$$

From equation (5)and equation (6), we get,

$$E_1 + E_2 = E_G - \left[E_{Cn} - E_{Vp}\right] \cdots\cdots\cdots\cdots\cdots\cdots \quad (7)$$

Also from band structure, $E_0 = E_1 + E_2 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (8)$

From equation (7) and equation (8), we get,

$$E_0 = E_G - \left[E_{Cn} - E_{Vp}\right] \cdots\cdots\cdots\cdots (9)$$

By adding equation (1) and (2), we get,

$$E_{Cn} - E_F + E_F - E_{Vp} = kT \ln\left[\frac{N_C}{N_D}\right] + kT \ln\left[\frac{N_V}{N_A}\right]$$

$$E_{Cn} - E_{Vp} = kT \ln\left[\frac{N_C}{N_D}\right] + kT \ln\left[\frac{N_V}{N_A}\right] \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (10)$$

Since, $np = e^{-(E_C - E_F)/kT} . N_C e^{-(E_F - E_V)/kT} . N_V$

$$n_i^2 = N_C N_V \, e^{-(E_C - E_V + E_F - E_F)/kT}$$

$$\frac{n_i^2}{(N_C N_V)} = e^{-(E_C - E_V)/kT}$$

$$\gg \qquad \frac{n_i^2}{(N_C N_V)} = e^{-\left(\frac{E_G}{kT}\right)} \qquad [\because E_C - E_V = E_G]$$

Taking ln on both sides we get,

$$\ln\left[\frac{n_i^2}{N_C N_V}\right] = -\left[\frac{E_G}{kT}\right]$$

$$kT \ln\left[\frac{N_C N_V}{n_i^2}\right] = E_G \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (11)$$

substituting the values of equation (10) and equation (11) in equation (9), we get,

$$E_0 = kT \ln\left[\frac{N_C N_V}{n_i^2}\right] - kT \ln\left[\frac{N_C}{N_D}\right] - kT \ln\left[\frac{N_V}{N_A}\right]$$

$$E_0 = kT \ln\left[\frac{N_C N_V}{n_i^2} \times \frac{N_D}{N_C} \times \frac{N_A}{N_V}\right]$$

$$E_0 = kT \ln\left[\frac{N_A N_D}{n_i^2}\right] \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (12)$$

Further for p-type, $p_{p_0} = N_A$, $n_{p0} = \frac{n_i^2}{N_A}$, $N_A = \frac{n_i^2}{n_{p0}}$

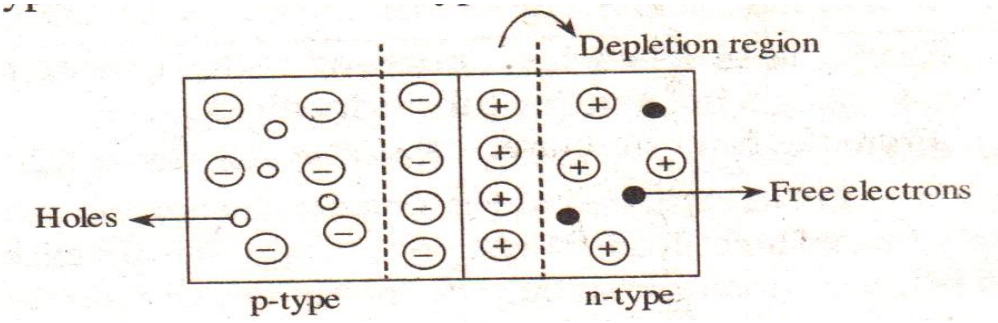
Further for N-type, $n_{n_0} = N_D$, $p_{n0} = \frac{n_i^2}{N_D}$, $N_D = \frac{n_i^2}{p_{n0}}$

Therefore $E_0 = kT \ln\left[\frac{n_{n0}}{n_{p0}}\right]$ and $E_0 = kT \ln\left[\frac{P_{p0}}{p_{n0}}\right]$

Where the subscript '0' indicate that the above relations are obtained under thermal conditions of equilibrium.

8. What do you understand by depletion region at pn junction? What is the effect of forward and reverse biasing of pn junction on the depletion region? Explain with necessary diagrams.

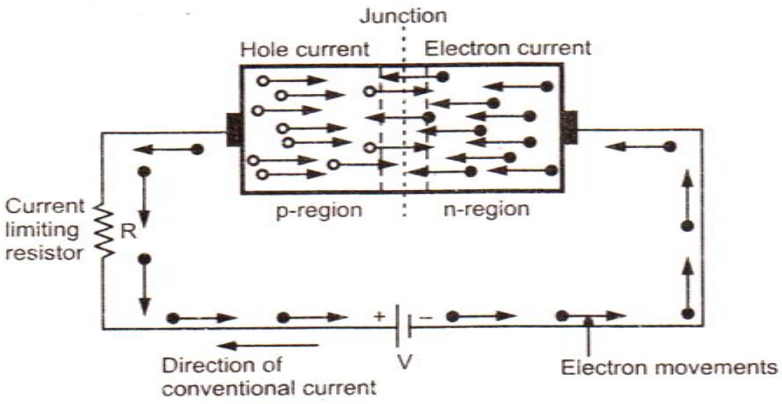
Ans: *Depletion region*: In a PN junction p-type consists of holes and n-type consists of electrons. Due to diffusion, the large number of holes from p-side diffuse to n-side and similarly, the large number of electrons from n-side diffuse to p-side.



Due to this displacement, p-side looses holes and forms a negative electric field to the left side of junction and n-side looses electrons and forms a positive electric field to the right side of the junction. Because of this large movement of holes and electrons, a barrier potential is developed across the junction. Finally, the holes will combine with free electrons and gets disappear leaving negative potential at p-side near the junction. Similarly the free electrons will combine with holes and gets disappear leaving positive potential at n-side near the junction. This region at the junction is known as depletion region.

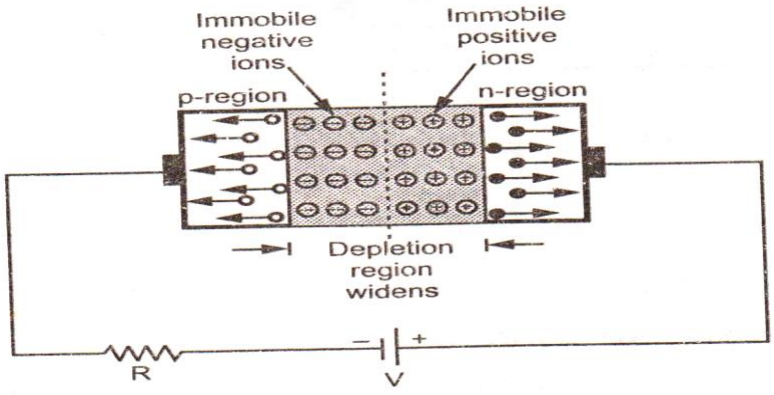
The thickness of depletion region is the order of few microns. Where, 1 micron=10^{-4}cm.

Forward bias:



In forward bias, the thickness of depletion layer is very thin because p-type is connected to positive terminal and the n-type is connected to the negative terminal. This causes the holes and electrons to move freely across the junction, hence resulting in a large current.

Reverse bias:



In reverse bias, as the p-type is connected to the negative terminal and n-type is connected to the positive terminal, the force of attraction takes place, so the holes from p-side and the electrons from n-side moves away from the junction, thus increasing the width of depletion region. This results in a very little current, almost equal to zero. Therefore, in reverse bias the thickness of the depletion region is large.

9. Explain about various current components in a forward biased pn junction diode.

Ans:

- When a p-n junction is forward biased a large forward current flows, which is mainly due to majority carriers. The depletion region near the junction is very very small, under forward biased condition.
- In forward biased condition holes get diffused into n side from p side while electrons get diffused into p-side from n side.
- So on p-side, the current carried by electrons which is diffusion current due to minority carriers, decreases exponentially with respect to distance measured from the junction. This current due to electrons, on p-side which are minority carriers is denoted as I_{np}.
- Similarly holes from p side diffuse into n-side carry current which decreases exponentially with respect to distance measured from the junction. This current due to holes on n-side, which are minority carriers is denoted as I_{pn}.

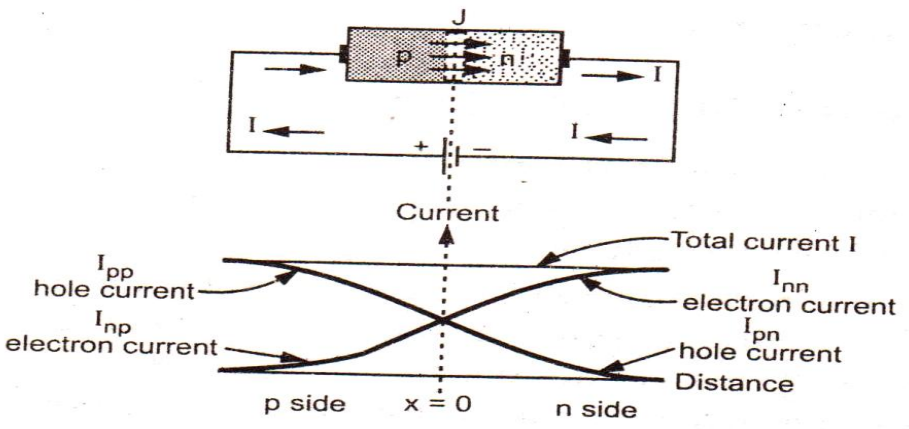


Fig: Current componets

- If distance is denoted by then,
  $I_{np}(x)$ = Current due to electrons in p side as a function of x
  $I_{pn}(x)$ = Current due to holes in n side as a function of x
- At the junction i.e. at x = 0, electrons crossing from n side to p side constitute a current, $I_{np}(0)$ in the same direction as holes crossing the junction from p side to n side constitute a current , $I_{pn}(0)$. Hence the current at the junction is the total conventional current I flowing through the circuit.

$\therefore \quad I = I_{pn}(0) + I_{np}(0)$

- But as the entire circuit is a series circuit, the total current must be maintained at I, independent of x. This indicates that on p side there exists one more current component which is due to holes on p side which are majority carriers. It is denoted by $I_{pp}(x)$.
  $I_{pp}(x)$ = current due to holes in p side
- Similarly on n side, there exists, there exists one more current component which is due to electrons on n side, which are the majority carriers. It is denoted by $I_{nn}(x)$.
  $I_{nn}(x)$ = Current due to electrons in n side.
- On p side the total current is $I = I_{pp}(x) + I_{np}(x)$
- On n side the total current is $I = I_{nn}(x) + I_{pn}(x)$

10. Define law of junction. Explain about the term cut-in voltage associated with pn junction diode. How do you obtain cut-in voltage from forward V-I characteristics?

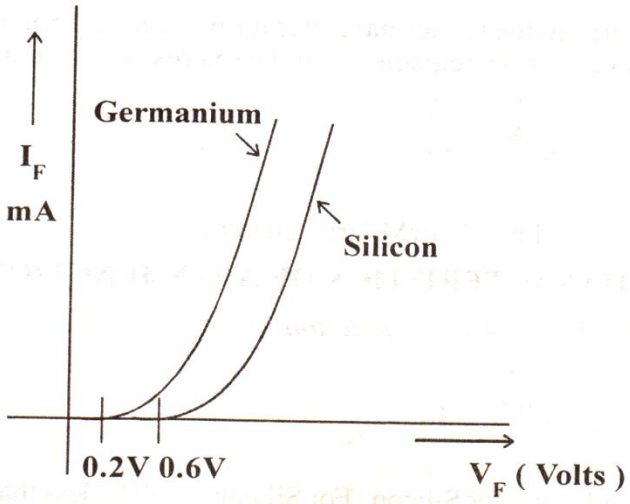
Ans: Law of Junction: This law states that for a forward biased junction diode the injected hole concentration $p_n(0)$ in the n-region increases over thermal equilibrium value P_{n_0}. It is given by,

$$p_n(0) = p_{n_0} e^{\frac{V}{V_T}}$$

Similarly for electron concentration, $n_p(0) = n_{p_0} e^{\frac{V}{V_T}}$

Cut-in voltage V_γ is the minimum bias voltage that should be applied across a diode for conduction to take place. The amount of current below V_γ is very small and above V_γ the current raises rapidly. Typically values of V_γ for germanium and silicon diodes are 0.2 V and 0.6V respectively.

The forward V-I characteristics of a junction diode are shown below.



Cut-in voltage can be obtained from the V-I characteristics by selecting a point on voltage axis where the current raises rapidly.

11.What are the applications of PN diode and Explain the volt-ampere characteristics of PN diode.

Ans: PN diode applications:

- Rectifiers in DC power supplies
- Switching in digital logic circuits
- Clippers in wave shaping circuits
- Clampers in TV receivers
- Diode gates
- Comparator

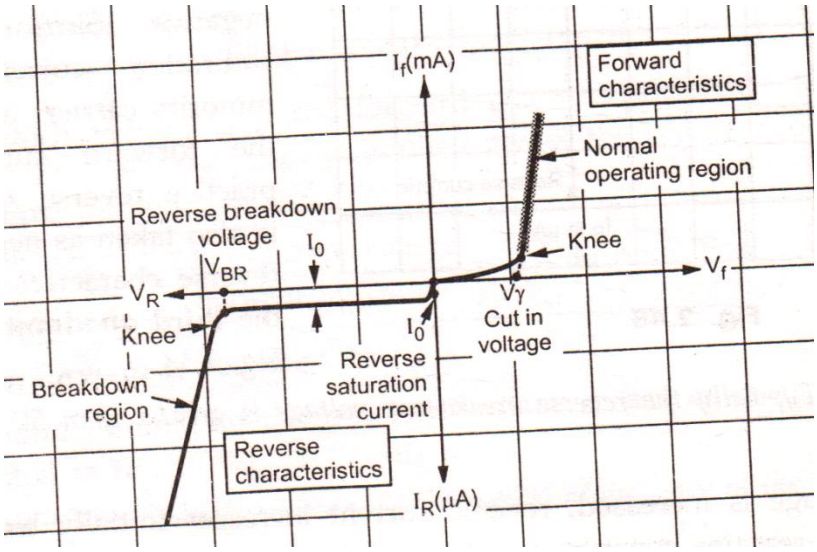


Fig: V-I Characteristics of a Diode

- ***In forward characteristics***, it is seen that initially forward current is small as long as the bias voltage is less than the barrier potential.
- At a certain voltage close to barrier potential, current increases rapidly.
- The voltage at which diode current starts increasing rapidly is called as cut-in voltage. It is denoted by V_γ.
- Below this voltage, current is less than 1% of maximum rated value of diode current.
- The cut-in voltage for germanium is about 0.2V while for silicon it is 0.6V.
- ***In* reverse *characteristics*** , reverse current increases initially as reverse voltage is increased. But after a certain voltage, the current remains constant equal to reverse saturation current I_0.
- The voltage at which breakdown occurs is called reverse breakdown voltage denoted as V_{BR}.
- Reverse current before the breakdown is very small and can be neglected practically.
- It is important to note that the breakdown voltage is much higher and practically diodes are not operated in the breakdown condition.

12. Explain the temperature dependence of V-I characteristics.

Ans: Dependency on V-I characteristics on temperature

The generation of electron hole pairs in semiconductors is increased due to the rise in temperature and which further leads to increase in their conductivity. Thus, the variation of current through the pn junction diode with temperature can be obtained using diode current equation i.e.,

$$I = I_0\left[e^{(V/\eta V_T)} - 1\right]$$

Where, $I =$ Diode current

I_0 = Diode reverse saturation current

V = External applied voltage to the diode

η = Constant = 1 for germanium

= 2 for silicon

V_T = Thermal voltage = $\frac{T}{11600}$

T = Temperature of diode junction(^{o}K)

For the diodes both germanium and silicon, the reverse saturation current I_0 increases approximately 7 percent/^{o}C. The reverse saturation current approximately doubles for every 10^{o}C rise in temperature. Since $(1.07)^{10} \approx 2$. Thus current I increases, if the temperature is increased at fixed voltage. By only reducing V, we can bring back current I to its original value. In order to maintain a constant current I value, the value of $\frac{dV}{dT}$ is found to be -2.5mV/^{o}C at room temperature for either germanium or silicon.

Basically, the value of cut-in voltage(or barrier voltage) is about 0.3V for germanium and 0.7 V for silicon. For both germanium and silicon diodes, the barrier voltage is decreased by 2mV/^{o}C. This is due to dependency of barrier voltage on temperature. Mathematically,

$$I_{02} = I_{01} \times 2^{(T_2 - T_1)/10}$$

Where, $I_{01}-$ Saturation current of the diode at temperature, T_1

I_{02} − Saturation current of the diode at temperature, T_2.

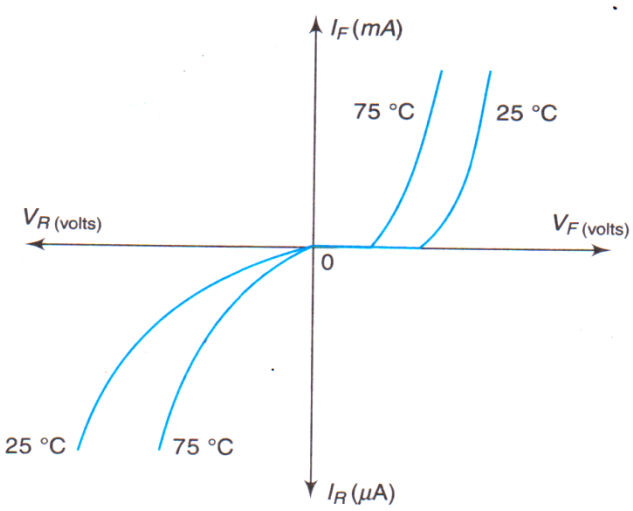


Fig: Effect of Temperature on the Diode charactristics

The effect of increased temperature on the pn junction diode characteristic curve is shown in figure. The maximum limit of temperature upto which a germanium and silicon diodes can used are 75^o and 175^oC respectively.

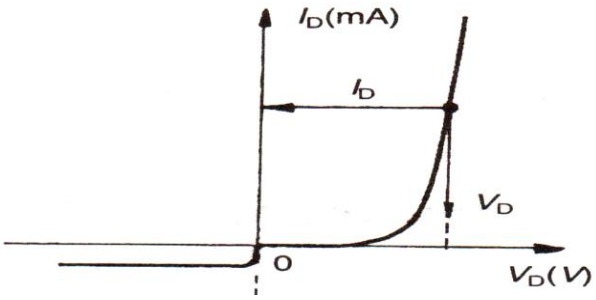
13. Explain about static and dynamic resistance in pn diode.

Ana: *DC or Static Resistance*

- The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the Corresponding levels of V_D and I_D as shown in Fig.(1) and applying the following Equation:

$$R_D = \frac{V_D}{I_D}$$

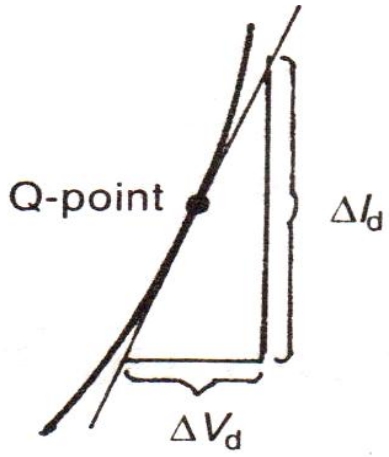
- The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few mill amperes).



Figure(1): Determining the dc resistance of a diode at a particular operating point.

AC or Dynamic Resistance

- It is obvious from above equation that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage. With no applied varying signal, the point of operation would be the *Q*-point determined by the applied dc levels as shown in fig(2).



Figure(2): determining the ac resistance at a *Q*-point

- A straight line drawn tangent to the curve through the *Q*-point as shown in Fig. 2 will define a particular change in voltage and current that can be used to determine the *ac* or *dynamic* resistance for this region of the diode characteristics. In equation form,

$$r_D = \frac{\Delta V_D}{\Delta I_D}$$

14. Write short notes on transition capacitance and Diffusion capacitance.

Ans: ***Transition capacitance:***

- Consider a reverse biased p-n junction diode as shown in figure.

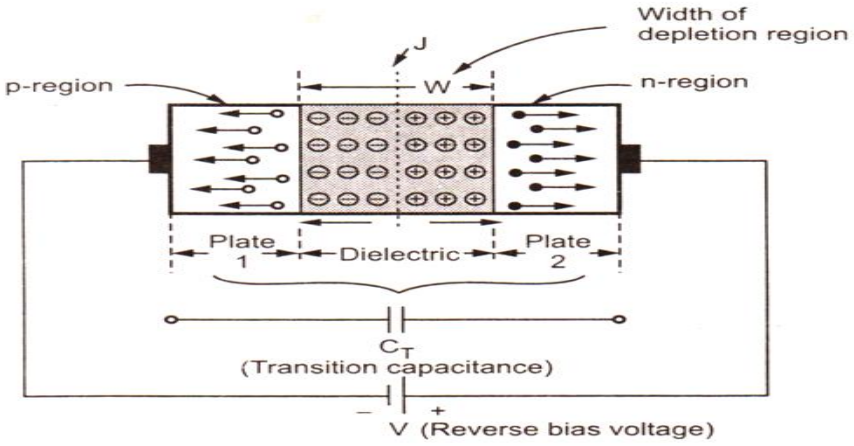


Fig: Transition capacitance in reverse biased condition

- When a diode is reversed biased, reverse current flows due to minority carriers.
- The width of the depletion region increases as reverse bias voltage increases.
- As the charged particles move away from the junction there exists a change in charge with respect to the applied reverse voltage.
- So change in charge dQ with respect to the change in voltage dV is nothing but a capacitive effect.
- Such a capacitance which into the picture under reverse biased condition is called *Transition capacitance or space charge capacitance* denoted as C_T.

$$C_T = \left|\frac{dQ}{dV}\right| = \frac{\varepsilon A}{W}$$

Where, dQ is the increases in charge caused by a change dV in voltage.

Diffusion Capacitance

- When a p-n junction is forward biased, the depletion layer almost completely disappears.
- The electrons move and stored in p-region and holes stored in n-region.
- As applied voltage increases, the amount of charge stored on both sides of junction also increases.
- It is observed that the charge stored varies directly as the applied forward bias voltage.
- This effect is similar to a capacitor in which amount of charge stored varies with applied voltage.

$$C_T = \frac{dQ}{dV} = \frac{Rate\ of\ change\ of\ charge\ at\ junction}{Rate\ of\ change\ of\ applied\ \ forward\ \ voltage}$$

- The flow of charge Q results in a diode current I is given by

$$I = \frac{Q}{\tau}$$

$$Q = I \times \tau \qquad \cdots\cdots (1)$$

Where τ is average life time of charge carrier

The diode current equation $I = I_0\left[e^{V/\eta V_T} - 1\right]$

The charge $Q = \left[I_0\left[e^{V/\eta V_T} - 1\right]\right]\tau$

Differentiating above equation with respect to V

$$\frac{dQ}{dV} = \frac{\tau I_0}{\eta V_T}\left[e^{V/\eta V_T}\right] \qquad \cdots\cdots\cdots\cdots\cdots (2)$$

From diode current equation $I = I_0 e^{V/\eta V_T} - I_0$

$$I + I_0 = I_0 e^{V/\eta V_T} \qquad \cdots\cdots\cdots (3)$$

Substitute equation (3) in equation (2)

$$\frac{dQ}{dV} = \frac{\tau}{\eta V_T}(I + I_0)$$

$$\frac{dQ}{dV} \approx \frac{\tau I}{\eta V_T} \qquad since\ I \gg I_0$$

Diffusion capacitance, $C_D = \frac{\tau I}{\eta V_T}$

15. Derive an expression for transition capacitance.

- Consider a p-n junction diode, the two sides of which are not equally doped.
- Assume that p-side is lightly doped and n side is heavily doped.
- If $N_A << N_D$, then $W_p >> W_n$.

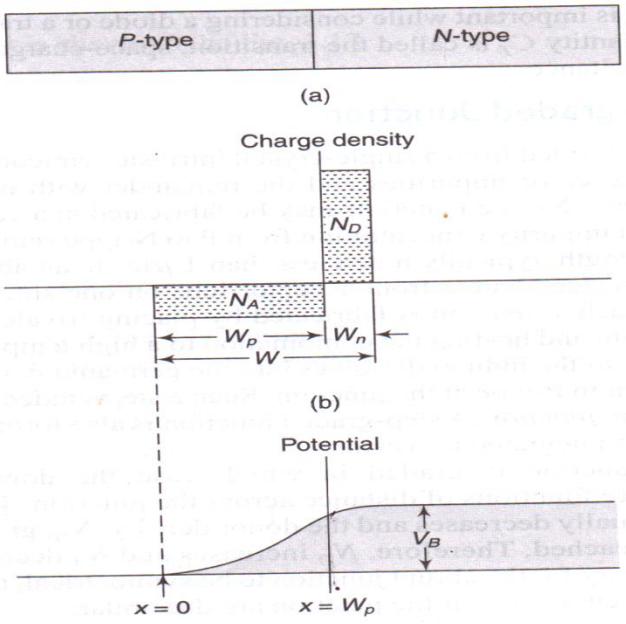


Fig: Unequally doped p-n junction diode

- Hence the width of depletion region on n-side is negligible small compared to width of depletion region on p-side.
- Hence the entire depletion region can be assumed to be on the p-side only
- The relationship between potential and charge density is given by poisson's equation,

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\varepsilon} \qquad \cdots\cdots\cdots\cdots (1)$$

Integrating equation (1) twice

$$\therefore\ V = \frac{qN_A}{\varepsilon}\frac{w^2}{2} \qquad \cdots\cdots\cdots\cdots\ (2)$$

At $x = w, V = V_B$ which is barrier potential

$$V_B = \frac{qN_A}{\varepsilon}\frac{w^2}{2} \qquad \cdots\cdots (3)$$

From the above expression it can be observed that $w \propto \sqrt{V_B}$

The width of barrier i.e depletion layer increases with applied reverse bias.

Differentiating equation (3) w.r.toV,

$$1 = \frac{1}{2}\frac{qN_A}{\varepsilon}\left[\frac{dw}{dV}\right]2w$$

$$\frac{dw}{dV} = \frac{\varepsilon}{qN_A w} \qquad \cdots\cdots (4)$$

If A is the area of cross section of the junction, then net charge Q in the distance *w* is

$$Q = no.of\ charged\ particles\ \times charge\ on\ each\ particle$$
$$= [N_A \times Volume\ ]q$$

$$= N_A\, AWq \qquad \cdots\cdots (5)$$

Differentiating equation (5) w.r.to V,

$$\frac{dQ}{dV_R} = N_A\, Aq \frac{dW}{dV}$$

$$= N_A\, Aq \frac{\varepsilon}{qN_A W}$$

$$C_T = \frac{\varepsilon A}{W}$$

16. Explain in brief about diode equivalent circuit.

Ans: An equivalent circuit is combination of elements, inserted in the place of a device without changing behavior of system.

Different equivalent circuit models of diode are given below.

- Piece wise linear model
- Simplified model
- Ideal Diode model

Piece wise linear model: Figure shows the V-I characteristics of a diode in piece wise linear model. The slope of straight line represents the reciprocal of a diode resistance, when the diode is ON. Whenever the voltage across the diode reaches V_γ then the diode will be ON.

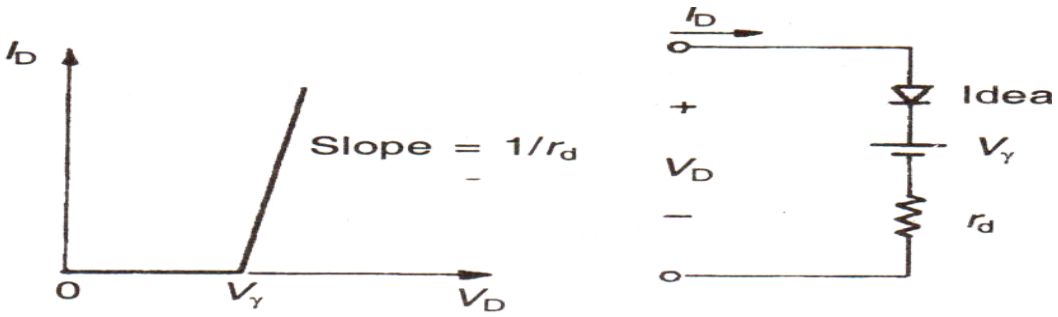


Fig: V-I Characteristics and its Equivalent Circuit of Piece Wise Linear Model

Simplified model: If we consider above piece wise linear model, the resistance r_d is practically smaller. So by removing the r_d, we get the diode equivalent in simplified model.

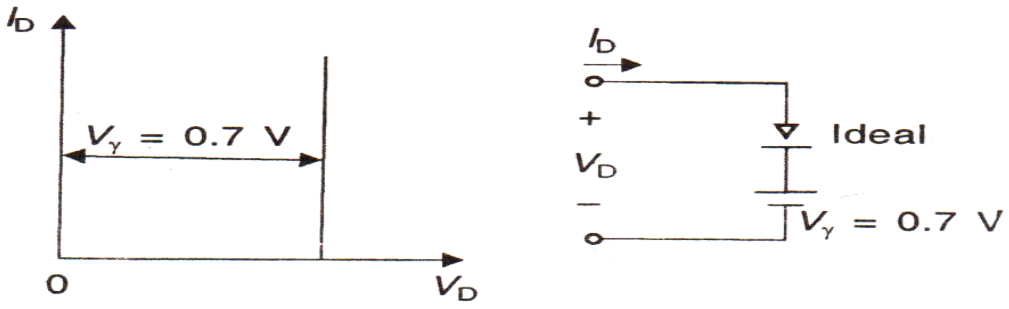


Fig: V-I Characteristics and its Equivalent Circuit of Simplified Model

Ideal Diode model: An ideal diode is the first and simplest approximation of a real diode. It has no forward voltage drop, no reverse current, and no breakdown. In fact, an ideal diode is only a theoretical approximation of a real diode. However, in a well defined circuit, a real diode behaves almost like an ideal diode because forward voltage across the diode is small as compared to the input and output voltages.

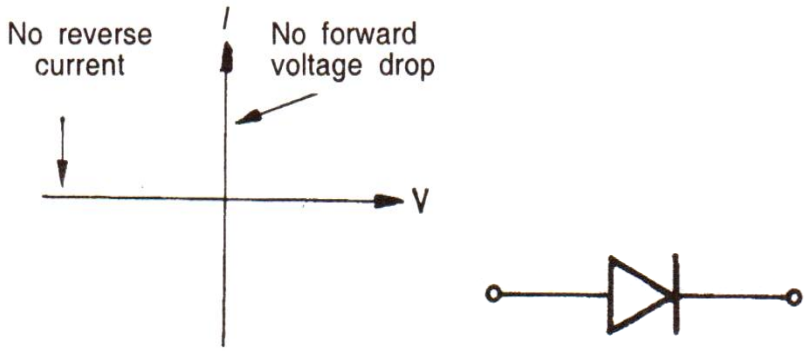


Fig: V-I Characteristics and its Equivalent Circuit of ideal Diode

17. Explain about breakdown mechanisms in semiconductor diodes.

A: **Avalanche breakdown**

- Though reverse current is not dependent on reverse voltage, if reverse voltage is increased, at a particular value, velocity of minority carriers increases.
- Due to kinetic energy associated with the minority carriers, more minority carriers are generated when there is collision of minority carriers with the atoms.
- The collision makes the electrons to break the covalent bonds.
- These electrons are available as minority carriers and get accelerated due to high reverse voltage.
- They again collide with another atoms to generate more minority carriers. This is called ***carrier multiplication***.
- Finally large number of minority carriers move across the junction, breaking the p-n junction.
- These large number of minority carriers give rise to a very high reverse current.
- This effect is called ***avalanche effect*** and the mechanism of destroying the junction is called reverse breakdown of a p-n junction.
- The voltage at which breakdown of a p-n junction occurs is called ***reverse breakdown voltage.***

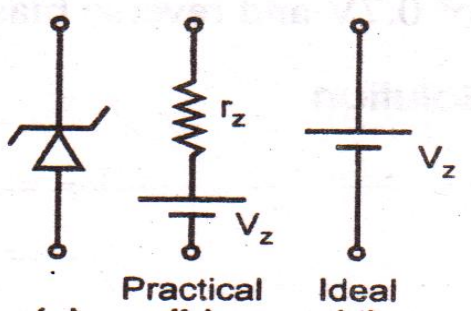
Zener breakdown

- When a p-n junction is heavily doped the depletion region is very narrow. So under reverse bias conditions, the electric field across the depletion layer is very intense.
- Such an intense field is enough to pull the electrons out of the valance bands of the stable atoms.
- So this is not due to the collision of carriers with atoms.
- Such a creation of free electrons is called zener effect.
- These minority carriers constitute very large current and mechanism is called zener breakdown.

18 Explain about Zener diode and its characteristics.

A **Zener diode**

- The diodes designed to work in breakdown region are called zener diode.
- It is heavily doped than ordinary diode.
- Operates in reverse breakdown region.
- It can be used as voltage regulator.



- When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but when a reverse voltage is applied to it the reverse saturation current remains fairly constant over a wide range of voltages.

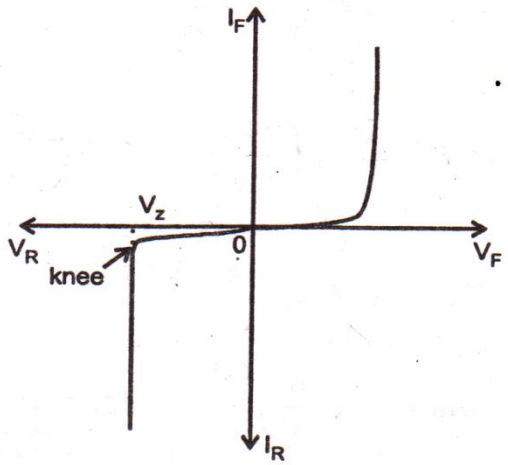


Fig: V-I Characteristics of a Zener diode

- Under forward bias condition, zener diode is same as that of ordinary pn diode.
- In reverse bias, as the reverse voltage V_R is increased the reverse saturation current remains extremely small up to knee of the curve.
- If the reverse voltage increased further, breakdown occurs and the current increase rapidly.
- The reverse voltage at which the breakdown occurs is known as reverse breakdown voltage.
- The breakdown voltage has a sharp knee, followed by an almost vertical increase in current, during which period the voltage across the device remains almost constant.
- Thus zener diode is most suited for voltage regulators.

Problems:

Problem 1

The mobility of free electrons and holes in pure germanium are 3800 and 1800 cm^2 /V-s respectively. The corresponding values for pure silicon are 1300 and 500 cm^2/V-s, respectively. Determine the values of intrinsic conductivity for both germanium and silicon. Assume $n_i = 2.5 \times 10^{13}$ cm^{-3} for germanium and $n_i = 1.5 \times 10^{10}$ cm^{-3} for silicon at room temperature.

Solution: (i) The intrinsic conductivity for germanium,

$$\sigma_i = qn_i(\mu_n + \mu_p)$$
$$= (1.6 \times 10^{-19})\ (2.5 \times 10^{13})\ (3800 + 1800)$$
$$= 0.0224 \text{ S/cm}$$

(ii) The intrinsic conductivity for silicon,

$$\sigma_i = qn_i\ (\mu_n + \mu_p)$$
$$= (1.6 \times 10^{-19})\ (1.5 \times 10^{10})\ (1300 + 500)$$
$$= 4.32 \times 10^{-6} \text{ S/cm}$$

Problem 2

In a P-type semiconductor, the Fermi level is 0.3 eV above the valance band at a room temperature of 300 °K. Determine the new position of the Fermi level for temperatures of (a) 350 °K and (b) 400 °K.

The Fermi level in a P-type material is given by

$$E_F = E_V + kT \ln \frac{N_V}{N_A}$$

Therefore, $(E_F - E_V) = kT \ln \frac{N_V}{N_A}$

At $T = 300$ °K, $0.3 = 300\ k \ln \frac{N_V}{N_A}$

(a) At $T = 350$ °K, $(E_{F1} - E_V) = 350k \ln \frac{N_V}{N_A}$

Hence, from the above equation

$$\frac{E_{F1} - E_V}{0.3} = \frac{350}{300}$$

Therefore, $E_{F1} - E_V = \frac{350}{300} \times 0.3 = 0.35$ eV

(b) At $T = 400$ °K, $(E_{F2} - E_V) = 400\ k \ln \frac{N_V}{N_A}$

Hence, from the above equation,

$$\frac{E_{F2} - E_V}{0.3} = \frac{400}{300}$$

Therefore, $E_{F2} - E_V = \frac{400}{300} \times 0.3 = 0.4$ eV

Problem 3

Find the concentration (densities) of holes and electrons in N-type Silicon at 300 °K, if the conductivity is 300 S/cm. Also find these values for P-type silicon. Given that for Silicon at 300 °K, $n_i = 1.5 \times 10^{10}/\text{cm}^3$, $\mu_n = 1300\ \text{cm}^2/\text{V-s}$ and $\mu_p = 500\ \text{cm}^2/\text{V-s}$.

Solution: (a) *Concentration in N-type Silicon*

The conductivity of an N-type Silicon is $\sigma = q\, n\, \mu_n$

Concentration of electrons, $n = \dfrac{\sigma}{q\,\mu_n}$

$$= \frac{300}{(1.6 \times 10^{-19})(1300)} = 1.442 \times 10^{18}\ \text{cm}^{-3}$$

Hence concentration of holes, $p = \dfrac{n_i^2}{n} = \dfrac{(1.5 \times 10^{10})^2}{1.442 \times 10^{18}} = 1.56 \times 10^{2}\ \text{cm}^{-3}$

(b) *Concentration in P-type silicon*

The conductivity of a P-type Silicon is $\sigma = qp\mu_p$

Hence, concentration of holes $p = \dfrac{\sigma}{q\mu_p}$

$$= \frac{300}{(1.6 \times 10^{-19})(500)} = 3.75 \times 10^{18}\ \text{cm}^{-3}$$

and concentration of electrons, $n = \dfrac{n_i^2}{p} = \dfrac{(1.5 \times 10^{10})^2}{3.75 \times 10^{18}} = 0.6 \times 10^{2}\ \text{cm}^{-3}$

Problem 4

(a) The resistivities of the P-region and N-region of a germanium diode are 6 Ω-cm and 4Ω-cm, respectively. Calculate the contact potential V_o and potential energy barrier E_o. (b) If the doping densities of both P and N-regions are doubled, determine V_o and E_o. Given that $q = 1.6 \times 10^{-19}$ C, $n_i = 2.5 \times 10^{13}/\text{cm}^3$, $\mu_p = 1800\ \text{cm}^2/\text{V-s}$, $\mu n = 3800\ \text{cm}^2/\text{V-s}$ and $V_T = 0.026$ V at 300 °K.

Solution: (a)Resistivity, $\rho = \dfrac{1}{\sigma} = \dfrac{1}{N_A\, q\, \mu_p}\ 6\,\Omega - \text{cm}$

Therefore, $N_A = \dfrac{1}{6q\mu_p} = \dfrac{1}{6 \times 1.6 \times 10^{-19} \times 1800} = 0.579 \times 10^{15}/\text{cm}^3$

Similarly, $N_D = \dfrac{1}{4q\mu_n} = \dfrac{1}{4 \times 1.6 \times 10^{-19} \times 3800} = 0.579 \times 10^{15}/\text{cm}^3$

Therefore, $V_o = V_T \ln \dfrac{N_D N_A}{n_i^2} = 0.026 \ln \dfrac{0.579 \times 0.411 \times 10^{30}}{(2.5 \times 10^{13})^2} = 0.1545$ V

Hence $E_0 = 0.1545$ eV

(b) $V_o = 0.026 \ln \dfrac{2 \times 0.579 \times 10^{15} \times 2 \times 0.411 \times 10^{15}}{(2.5 \times 10^{13})^2} = 0.1906$ V

Therefore, $E_0 = 0.1906$ eV

Problem5.

In the case of an open circuited p-n junction, the acceptor atom concentration is $2.5\times10^{16}/m^3$, donor atom concentration is $2.5\times10^{22}/m^3$ and intrinsic concentration is $2.5\times10^{19}/m^3$. Determine the value of the contact difference of potential.

Sol: $N_A = 2.5 \times 10^{16}/\mathrm{m}^3$

$N_D = 2.5 \times 10^{22}/\mathrm{m}^3$

$n_i = 2.5 \times 10^{19}/\mathrm{m}^3$

Contact potential $V_J = V_T \ln\left[\frac{N_A N_D}{n_i^2}\right]$

Assume $V_T = 26mV$

$$V_J = 26 \times 10^{-3} \ln\left[\frac{2.5\times10^{16}\times2.5\times10^{22}}{(2.5\times10^{19})^2}\right]$$

$$= 0V$$

Problem6.

A diode operating at 300K at a forward voltage of 0.4V carriers a current of 10mA. When voltage is changed to 0.42V the current becomes thrice. Calculate the value of reverse leakage current and η for the diode(assume V_T = 26 mV).

Sol: Given data:

$T = 300^0K$

V_1= 0.4V

I_1 = 10mA

V_2= 0.42V

I_2= 30 mA (given the current becomes thrice)

V_T = 26mV

To find: I_0 = ? η= ?

The expression for diode current is given by

$$I = I_0\left[e^{V/\eta V_T} - 1\right]$$

For V_1= 0.4V, I_1 = 10mA and V_T = 26mV, we get,

$$10 \times 10^{-3} = I_0\left[e^{0.4/\eta\times26\times10^{-3}} - 1\right]$$

$$= I_0\left[e^{\frac{400}{26\eta}} - 1\right] \qquad since \quad e^{\frac{400}{26\eta}} >> 1$$

$$10 \times 10^{-3} = I_0\, e^{\frac{400}{26\eta}} \qquad \cdots\cdots\cdots \quad (1)$$

For V_2= 0.42V, I_2 = 30mA and V_T = 26mV, we get,

$$30 \times 10^{-3} = I_0\left[e^{0.42/\eta \times 26 \times 10^{-3}} - 1\right]$$

$$= I_0\left[e^{\frac{420}{26\eta}} - 1\right] \qquad since \quad e^{\frac{400}{26\eta}} >> 1$$

$$30 \times 10^{-3} = I_0 e^{\frac{420}{26\eta}} \qquad \cdots\cdots\cdots \quad (2)$$

Dividing equation (2) with equation (1), we get,

$$\frac{30\times10^{-3}}{10\times10^{-3}} = \frac{I_0 e^{\frac{420}{26\eta}}}{I_0\, e^{\frac{400}{26\eta}}}$$

$$3 = e^{\frac{20}{26\eta}}$$

$$3 = e^{\frac{10}{13\eta}}$$

$$\frac{10}{13\eta} = ln3 = 1.099$$

$$\therefore \eta = 0.7$$

Then , substituting the above η value in equation (1), we get,

$$10 \times 10^{-3} = I_0\, e^{\frac{400}{26\times0.7}}$$

$$\therefore I_0 = 2.85\, pAms$$

Problem7.
A pn junction diode has a reverse saturation current of 30 µA at a temperature of 125^0 C. At the same temperature, find the dynamic resistance for 0.2 V bias in forward and reverse direction.
Sol: Given data:

$$I_0 = 30\mu A$$

$$T = 125^0 C$$

$$V_f = 0.2\ (forward\ bias)$$

$-V_f = -0.2\ (reverse\ bias)$

To find:

r_f =?

r_r =?

Consider **η** =2 for silicon

We know that, $V_T = \frac{T}{11600} = \frac{398}{11600} = 34.3 \times 10^{-3} V \quad [since\ T = 125 + 273 = 398^0 K]$

Forward dynamic resistance $r_f = \frac{\eta V_T}{I_0 e^{V/\eta V_T}} = \frac{2 \times 34.3 \times 10^{-3}}{30 \times 10^{-6} \times e^{\frac{0.2}{2 \times 34.3 \times 10^{-3}}}} = 123.9\Omega$

Reverse dynamic resistance $r_r = \frac{\eta V_T}{I_0 e^{-V/\eta V_T}} = \frac{2 \times 34.3 \times 10^{-3}}{30 \times 10^{-6} \times e^{\frac{-0.2}{2 \times 34.3 \times 10^{-3}}}} = 42.18K\Omega$

Diode Applications, Special Diodes

1. **Draw the block diagram of RPS. What are the important characteristics of a Rectifier circuit?**

Ans:

- For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c. voltages.
- The process of converting a.c. voltage into d.c. voltage is called as rectification. This is achieved with i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulator circuits.
- These elements constitute d.c. regulated power supply shown in the figure below.

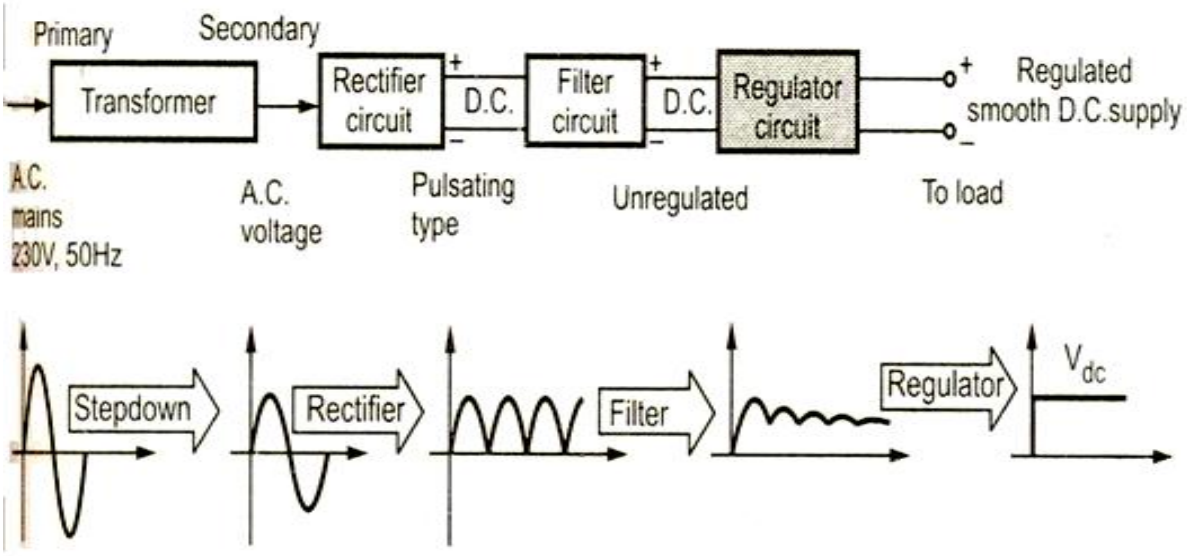


Fig. Block diagram of Regulated D.C. Power Supply

Stepdown Transformer: It steps down the high voltage A.C mains to low voltage A.C

Bridge Rectifier: It converts A.C to D.C but the D.C output is varying.

Filter: It will smooth the D.C from varying greatly to a small ripple.

Regulator: It eliminates the ripple by setting D.C output to a fixed voltage.

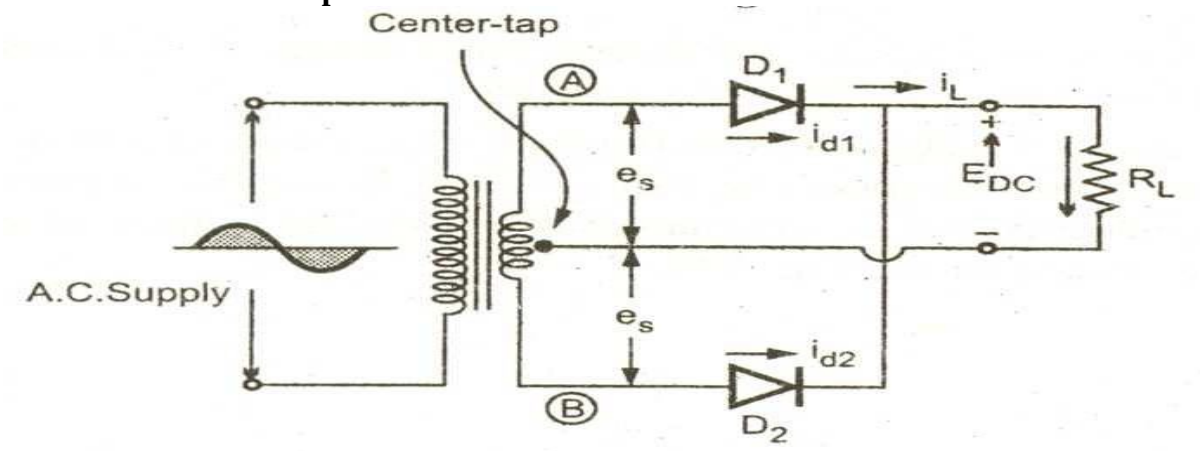
Characteristics of a Rectifier circuit

- The most important consideration in designing a rectifier is the unidirectional output voltage. Rectifier enable minimum operable DC voltage at the rated current.
- The regulations of rectifier circuit are also good i.e.,0.1%.
- The rectifier is protected in the event of short circuit on the load side.
- Over voltage protection is incorporated.
- The response of rectifier to the temperature changes is minimum.
- Transient response of this rectifier circuit is faster i.e., in μsec.

2. Draw the circuit diagram of a FWR, a) With centre tap connection and

b) Bridge connection and explain its operation.

Ans: FWR with centre tap connection



- The individual diode currents and the load current waveforms are shown in figure below:

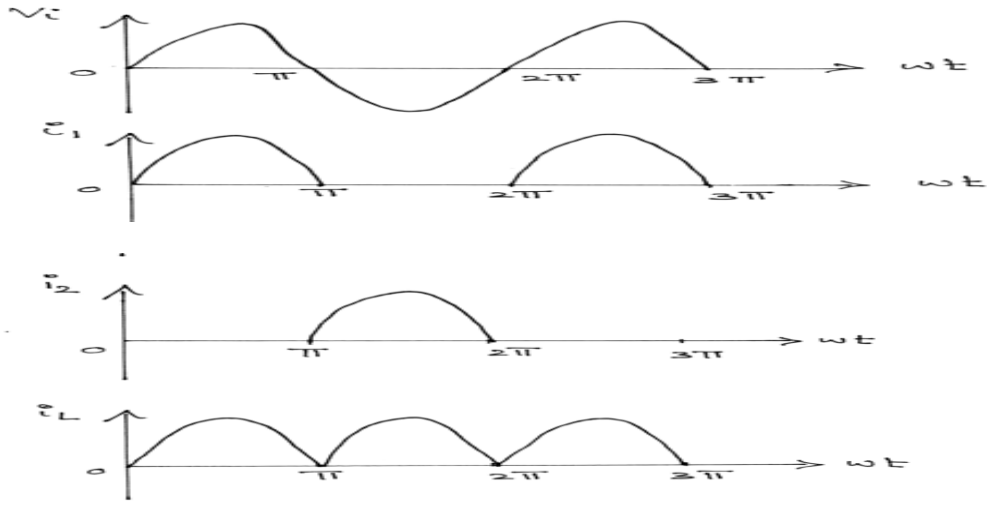


Fig. The input voltage, the individual diode currents and the load current waveforms.

Operation:

- During positive half of the input signal, anode of diode D_1 becomes positive and at the same time the anode of diode D_2 becomes negative. Hence D_1 conducts and D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.
- During the negative half cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage.
- It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

Bridge rectifier

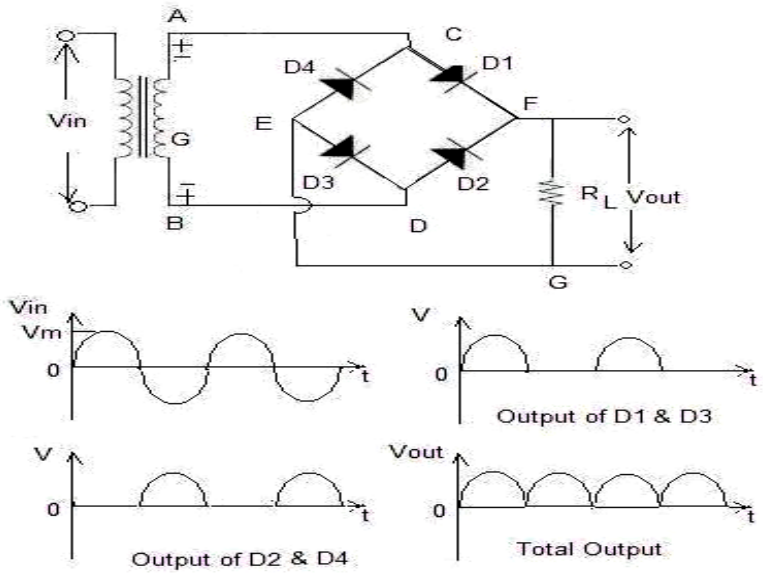


Fig. Bridge rectifier circuit and waveforms

Operation:

- For the positive half cycle of the input ac voltage diodes D_1 and D_3 conduct, whereas diodes D_2 and D_4 do not conduct. The conducting diodes will be in series through the load resistance R_L, so the load current flows through the R_L.
- During the negative half cycle of the input ac voltage diodes D_2 and D_4 conduct, whereas diodes D_1 and D_3 do not conduct. The conducting diodes D_2 and D_4 will be in series through the load resistance R_L and the current flows through the R_L, in the same direction as in the previous half cycle. Thus a bidirectional wave is converted into a unidirectional wave.

3. Define the terms as referred to FWR circuit.
(i) PIV
(ii) Average DC voltage
(iii) RMS current
(iv) Ripple factor
(v) Form factor
(vi) Peak factor

Ans: (i) PIV: Peak Inverse Voltage is the maximum possible voltage across a diode when it is reverse biased. Consider that diode D_1 is in the forward biased i.e., conducting and diode D_2 is reverse biased i.e., non-conducting. In this case a voltage V_m is developed across the load resistor R_L. Now the voltage across diode D_2 is the sum of the voltages across load resistor R_L and voltage across the lower half of transformer secondary V_m. Hence PIV of diode $D_2 = V_m + V_m = 2V_m$. Similarly PIV of diode D_1 is $2V_m$.

(ii) Average DC voltage: The dc output voltage is given by

$$V_{dc} = I_{dc}\, R_L = \frac{2I_m R_L}{л}$$

$$\frac{2}{л} \times \frac{V_m R_L}{R_L}$$

$$V_{dc} = \frac{2V_m}{л}$$

(iii) R.M.S current:

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

(iv) Ripple Factor (γ) : It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

The ripple factor, γ is given by $\gamma = \sqrt{\left[\frac{I_{rms}}{I_{dc}}\right]^2 - 1}$ or $\gamma = \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1}$

$$\gamma = \sqrt{\left[\frac{I_m}{\sqrt{2}} \times \frac{л}{2I_m}\right]^2 - 1}$$

$$= \sqrt{\left[\frac{л}{2\sqrt{2}}\right]^2 - 1}$$

$$\gamma = 0.482$$

(v) Form factor: In general, form factor is defined as

$$\text{Form factor} = \frac{\text{rms voltage}}{\text{average value}} = \frac{V_{rms}}{V_{DC}} = \frac{\frac{V_m}{\sqrt{2}}}{\frac{2V_m}{л}} = 1.11 \text{ For FWR}$$

(vi) Peak factor: In general, peak factor is defined as

$$\text{Peak factor} = \frac{\text{peak voltage}}{\text{rms voltage}} = \frac{V_m}{\frac{V_m}{\sqrt{2}}} = \sqrt{2} = 1.414 \text{ for FWR}$$

4. Derive the expression for the ripple factor of HWR and FWR.

Ans: Ripple Factor (γ) **:** It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

$$\gamma = \frac{V'rms}{V_{dc}}$$

$$V'rms = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\gamma = \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1}$$

For Half wave rectifier, ripple factor $\gamma = \sqrt{\left[\frac{I_{rms}}{I_{dc}}\right]^2 - 1}$ or $\gamma = \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1}$

$$= \sqrt{\left[\frac{I_m/2}{I_m/\pi}\right]^2 - 1}$$

$$= \sqrt{\left[\frac{\pi}{2}\right]^2 - 1}$$

$$= 1.21$$

For Full wave rectifier, ripple factor $\gamma = \sqrt{\left[\frac{I_{rms}}{I_{dc}}\right]^2 - 1}$ or $\gamma = \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1}$

$$\gamma = \sqrt{\left[\frac{I_m}{\sqrt{2}} \times \frac{\pi}{2I_m}\right]^2 - 1}$$

$$= \sqrt{\left[\frac{\pi}{2\sqrt{2}}\right]^2 - 1}$$

$$\gamma = 0.482$$

5. Compare Rectifier circuits:

Ans:

S.No.	Parameter	Half wave	Full Wave	Bridge
1	Number of Diodes	1	2	4
2	Average dc current, I_{dc}	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
3	Average dc voltage, V_{dc}	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
4	RMS current, I_{rms}	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
5	DC Power output, P_{dc}	$\frac{I_m^2 R_L}{\pi^2}$	$\frac{4I_m^2 R_L}{\pi^2}$	$\frac{4I_m^2 R_L}{\pi^2}$
6	AC Power input, P_{ac}	$\frac{I_m^2(R_L + R_f + R_s)}{4}$	$\frac{I_m^2(R_L + R_f + R_s)}{2}$	$\frac{I_m^2(R_L + 2R_f + R_s)}{2}$
7	Max. rectifier efficiency(η)	40.6%	81.2%	81.2%
8	Ripple factor (γ)	1.21	0.482	0.482
9	PIV	V_m	$2V_m$	V_m
10	TUF	0.287	0.693	0.812
11	Max. load current (I_m)	$\frac{V_m}{R_L + R_f + R_s}$	$\frac{V_m}{R_L + R_f + R_s}$	$\frac{V_m}{R_L + 2R_f + R_s}$
12	Ripple frequency	f	2f	f

6. Explain the principle of operation of HWR with and without capacitor input filter and the waveforms.

Ans:

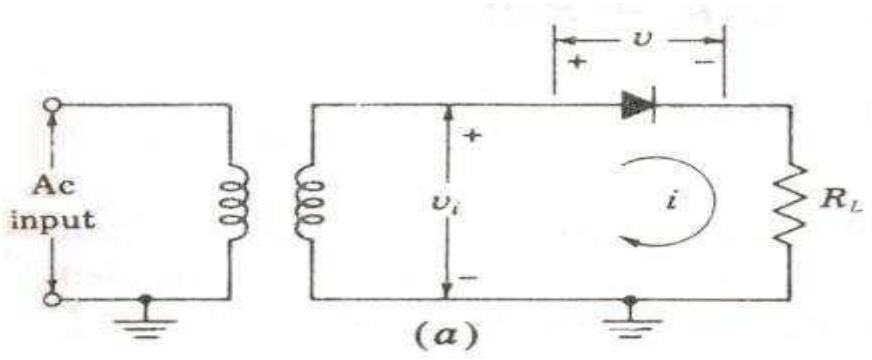
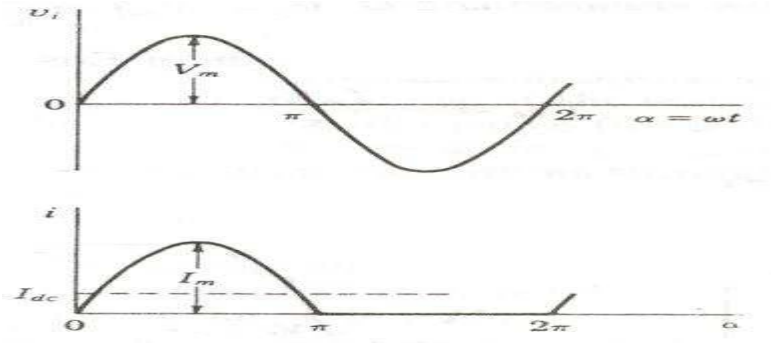


Fig. HWR without capacitor filter



Operation:

- For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across R_L. The waveform of the diode current (or) load current is shown in figure.
- For the negative half-cycle of input, the diode D is reverse biased and hence it does not conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half-cycle no power is delivered to the load.

HWR with capacitor input filter:

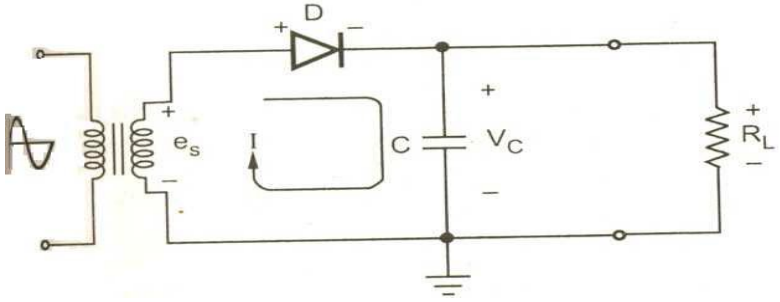


Fig. HWR with capacitor filter.

Operation:

- During, the positive quarter cycle of the ac input signal, the diode D is forward biased and hence it conducts. This quickly charges the capacitor C to peak value of input voltage V_m. Practically the capacitor charge (V_m-V_γ) due to diode forward voltage drop.
- When the input starts decreasing below its peak value, the capacitor remains charged at V_m and the ideal diode gets reverse biased. This is because the capacitor voltage which is cathode voltage of diode becomes more positive than anode.
- Therefore, during the entire negative half cycle and some part of the next positive half cycle, capacitor discharges through R_L. The discharging of capacitor is decided by R_LC, time constant which is very large and hence the capacitor discharge very little from Vm.
- In the next positive half cycle, when the input signal becomes more than the capacitor voltage, he diode becomes forward biased and charges the capacitor C back to V_m. The output waveform is shown in figure below:

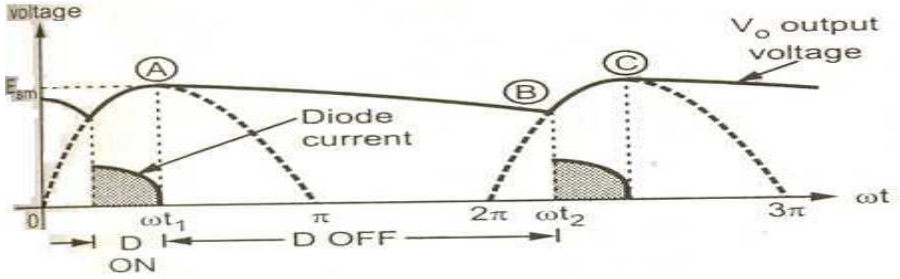


Fig. HWR output with capacitor filter.

- The discharging if the capacitor is from A to B, the diode remains non-conducting. The diode conducts only from B to C and the capacitor charges.

7. Derive the ripple factor of capacitor filter. (or) For a FWR with shunt capacitance filter derive expression for ripple factor using approximate analysis.

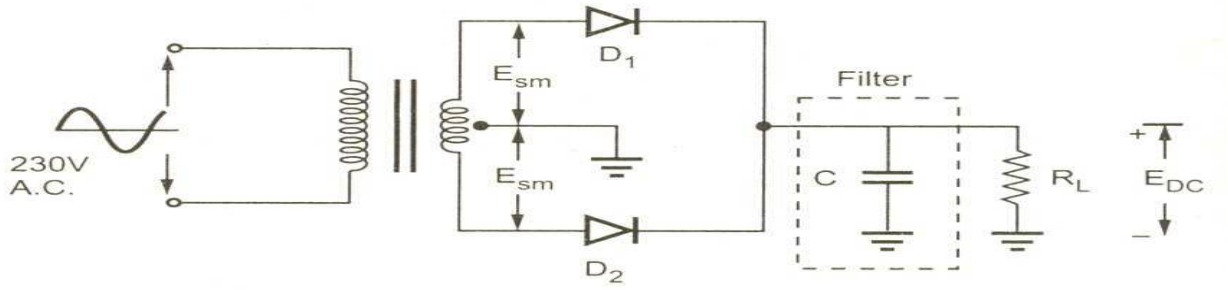


Fig. Full-wave rectifier with capacitor filter

Operation:

- During the positive quarter cycle of the ac input signal, the diode D_1 is forward biased, the capacitor C gets charges through forward bias diode D_1 to the peak value of input voltage Vm.
- In the next quarter cycle from $\frac{л}{2}$ to л the capacitor starts discharging through R_L, because once the capacitor gets charges to V_m, the diode D_1 gets reverse biased and stops conducting, so during the period from $\frac{л}{2}$ to л the capacitor C supplies the load current.

- In the next quarter half cycle, that is, л to $\frac{3л}{2}$ of the rectified output voltage, if the input voltage exceeds the capacitor voltage, making D_2 forward biased, this charges the capacitor back In the next quarter half cycle, that is, from $\frac{3л}{2}$ to 2л , the diode gets reverse biased and the capacitor supplies the load current.In FWR, as the time required by the capacitor to charge is very small and it discharges very little due to large time constant, hence ripple in the output gets reduced considerably.
- The output waveform is shown in figure below:

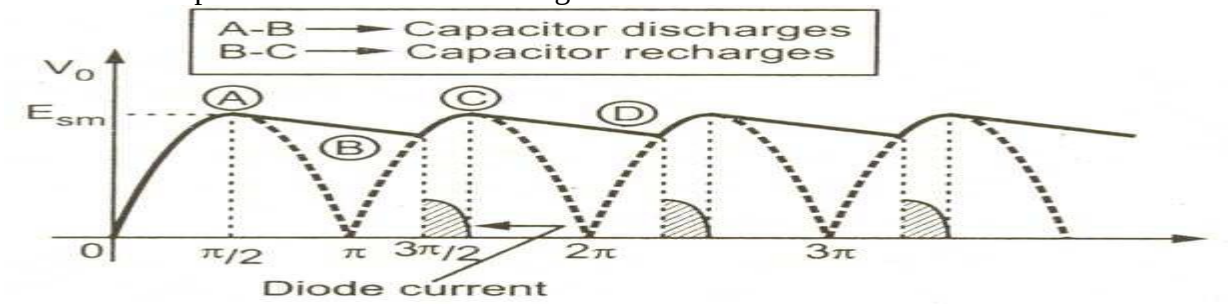
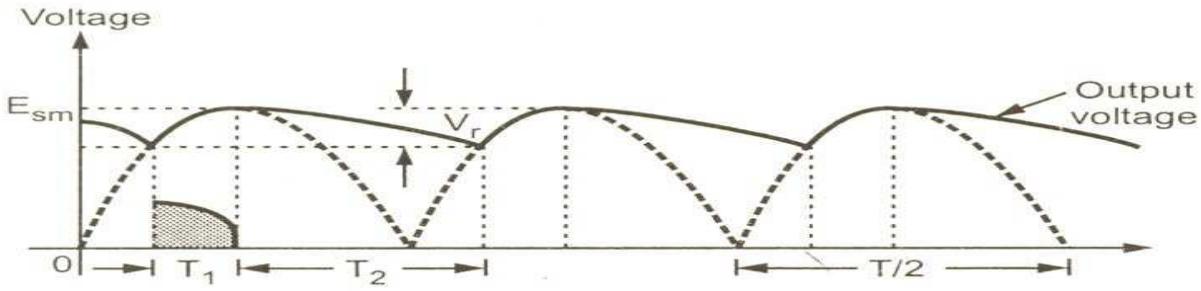


Fig. FWR output with capacitor filter.

Expression for Ripple factor:



Let, T = time period of the ac input voltage
T/2= half of the time period
T_1 = time for which diode is conducting
T_2 = time for which diode is non-conducting
During time T_1, capacitor gets charged and this process is quick. During time T_2, capacitor gets discharged through R_L. As time constant R_L C is very large, discharging process is very slow and hence $T_2 >> T_1$.
Let V_r be the peak to peak value of ripple voltage, which is assumed to be triangular as shown in the figure below:

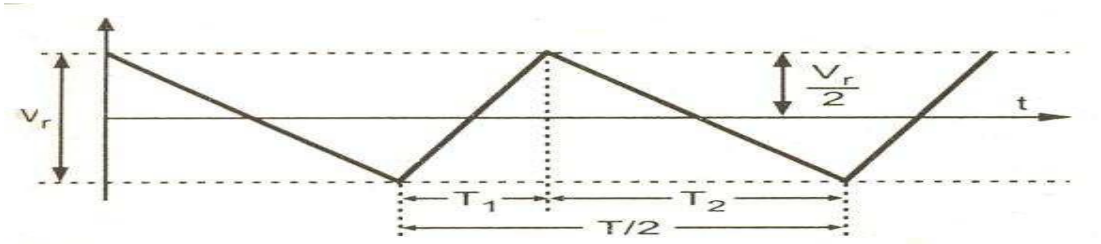


Fig. Triangular approximation of ripple

It is known mathematically that the rms value of such a triangular waveform is,

$$V_{rms} = \frac{V_r}{2\sqrt{3}}$$

During the time interval T_2, the capacitor C is discharging through the load resistance R_L.

The charge lost is, $Q = CV_r$ But $i = \frac{dQ}{dt}$

$$\therefore Q = \int_0^{T_2} idt = I_{DC}T_2$$

As integration gives average (or) dc value, hence $I_{dc} . T_2 = C . V_r$

$$\therefore V_r = \frac{I_{dc} T_2}{C} \quad \text{but } T_1+T_2 = T/2$$

Normally, $T_2 >> T_1$, $\therefore T_1+T_2 \approx T_1 = T/2$ where T=1/f

$$\therefore V_r = \frac{I_{dc}}{C}\left(\frac{T}{2}\right) = \frac{I_{dc} T}{2C} = \frac{I_{dc}}{2fC}$$

But $I_{DC} = \frac{V_{DC}}{R_L}$, $\therefore V_r = \frac{V_{DC}}{2fCR_L}$ = peak to peak ripple voltage

$$\text{Ripple factor} = \frac{V_{rms}}{V_{Dc}} = \frac{\frac{V_{DC}}{2fCR_L}}{2\sqrt{3}} \times \frac{1}{V_{DC}} \qquad [\therefore V_{rms} = \frac{V_r}{2\sqrt{3}}]$$

$$\therefore \text{Ripple factor} = \frac{1}{4\sqrt{3}fCR_L}$$

8. Draw the circuit diagram of FWR with inductor filter and explain its operation.

Ans: Full-wave rectifier with series inductor filter:

A FWR with series inductor filter is shown in figure.

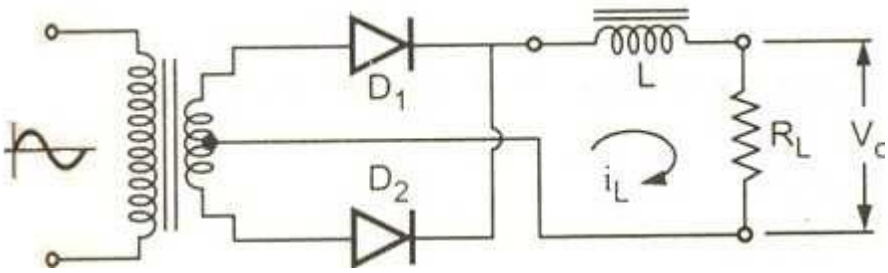


FIG. FWR with series inductor filter.

- In the positive half cycle of the secondary voltage of the transformer, the diode D_1 is forward biased. Hence the current flows through D_1, L & R_L.
- While in the negative half cycle, the diode D_1 is reverse biased while diode D_2 is forware biased. Hence the current flows through D_2, L & R_L. Hence we get unidirectional current through R_L.
- Due to inductor L , which opposes change in current , it tries to make the output smooth by opposing the ripple content in the output.
- In order to determine the ripple and its relation to 'L' the current flowing through the FWR is represented by fourier series form.
- Fourier series for the load current for FWR as,

$$i_L = I_m\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t - - - -\right]$$

Neglecting higher order harmonics we get,

$$i_L = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi}\cos 2\omega t \text{ ---------- } (1)$$

Neglecting diode forward resistance and the choke resistance and transformer secondary resistance, we can write the dc component of current as

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi R_L} \quad \text{---------- (2)}$$

While the second harmonic component represents ac component or ripple present and can be written as

$$I_m = \frac{V_m}{Z} \quad \text{---------- (3)}$$

Where $Z = R_L + J\,2X_L = \sqrt{R_L^2 + (2\omega L)^2} = \sqrt{R_L^2 + 4\omega^2 L^2}$

$$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}} \quad \text{---------- (4)}$$

Substitute equation (4) in equation (1)

$$i_L = \frac{2I_m}{\pi} - \frac{4V_m \cos(2\omega t - \varphi)}{3\pi\sqrt{R_L^2 + 4\omega^2 L^2}} \quad \text{---------- (5)}$$

i.e i_L = dc component + ac component

where φ is the angle by which the load current lags behind the voltage.

Expression for the ripple factor

Ripple factor $\gamma = \frac{I_{rms}}{I_{DC}}$ ---------- (6)

Where $I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{4V_m}{3\sqrt{2}\pi\sqrt{R_L^2 + 4\omega^2 L^2}}$ and $I_{DC} = \frac{2V_m}{\pi R_L}$

Substitute above two equations in equation (6)

$$\text{Ripple factor } \gamma = \frac{\frac{4V_m}{3\sqrt{2}\pi\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}} = \frac{2}{3\sqrt{2}} \times \frac{1}{\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

Initially on no load condition, $R_L \rightarrow \infty$ and hence $\frac{4\omega^2 L^2}{R_L^2} \rightarrow 0$

$$\gamma = \frac{2}{3\sqrt{2}} = 0.472$$

This is very close to normal FWR without filtering. So neglecting 1 we get

$$\text{Ripple factor } \gamma = \frac{2}{3\sqrt{2}} \times \frac{1}{\sqrt{\frac{4\omega^2 L^2}{R_L^2}}}$$

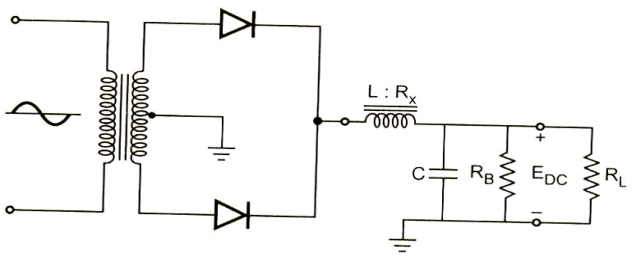
$$\text{For FWR } \gamma = \frac{R_L}{3\sqrt{2}\omega L}$$

So as load changes, ripple changes which is inversely proportional to the value of the inductor.

9. Derive the expression for ripple factor for FWR with L-section filter. Explain the necessity of a bleeder resistor.

Ans:

- In inductor filter the ripple factor is directly proportional to load resistance and in capacitor filter the ripple factor is indirectly proportional to load resistance.
- If we combine the above two filters, then the ripple factor becomes almost independent of load resistance.



R_X ⟶ dc winding resistance of the choke, R_B ⟶ Bleeder resistance

Ripple factor derivation

- The analysis of the LC filter circuit is based on the following assumptions.
- $X_L >> R_X$, $X_L >> X_C$, $R >> X_C$, $R >> R_X$. where $R = R_B \| R_L$.
- Since the filter elements, L & C are having resonable large values, the reactances X_L of the inductance L at 2ω i.e. $X_L = 2\omega L$ is much larger than R_X.
- Also the reactance X_L is much larger than the reactance of C, X_C at 2ω as $X_C = \frac{1}{2\omega C}$
- The input voltage e_{in} , to the LC filter is the output voltage of the FWR using fourier series, the input voltage "e_{in}" can be written as

$$e_{in} = V_m\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t - - - -\right]$$

The first term $\frac{2V_m}{л}$ indicates the DC output voltage of the rectifier. Remaining terms indicate ripples.

$$e_{in} \approx V_m\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t\right]$$

$$V_{DC} = \frac{2V_m}{л}$$

The impedance Z_2 of the filter circuit for 2nd harmonic component of input , i.e. at 2ω will be

$$Z_2 = R_X + 2J\omega L + \left[\frac{1}{2J\omega C} \| R\right]$$

As per assumptions $|Z_2| = 2\omega L$

Second harmonic component of the current in the filter circuit will be

$$I_{2m} = \frac{\frac{4V_m}{3л}}{Z_2} \approx \frac{\frac{4V_m}{3л}}{2\omega L}$$

The second harmonic voltage across the load is

$$V_{2m} = I_{2m}\frac{1}{2\omega C} = \frac{\frac{4V_m}{3л}}{2\omega L} \times \frac{1}{2\omega C} = \frac{V_m}{3\pi\omega^2 LC}$$

$$\therefore V_{2rms} = \frac{V_{2m}}{\sqrt{2}} = \frac{V_m}{3\sqrt{2}\pi\omega^2 LC}$$

Ripple factor $\gamma = \frac{V_{2rms}}{V_{DC}} = \frac{V_m}{3\sqrt{2}\pi\omega^2 LC} \times \frac{\pi}{2V_m}$

Ripple factor $\gamma = \frac{1}{6\sqrt{2}\omega^2 LC}$

It is seen that the ripple factor for LC filter does't depend upon the load resistance unlike the capacitor filtor.

The necessity of Bleeder Resistance R_B:

- The basic requirement of this filter circuit is that the current through the choke must be continuous and not interrupted.
- An interrupted current through the choke may develop a large back emf which may be in excess of PIV rating of the diodes and or maximum voltage rating of the capacitor.
- Thus this back emf is harmful to the diodes and capacitor.
- To eliminate the back emf developed across the choke, the current through it must be maintained continuous.
- This is assured by connecting a bleeder resistance, R_B across the output.

10. Derive the ripple factor of л-filter with neat sketch. (or) Discuss a FWR with л-filter.

Ans:

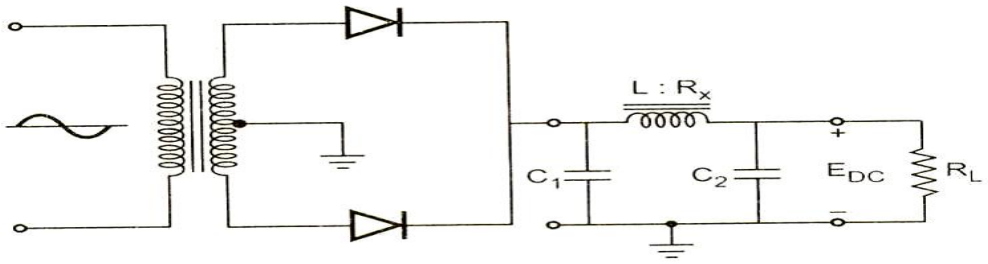


Fig. Π-section Filter.

- It consists of an inductance L with a dc winding resistance as R_x and two capacitors C1 and C2. The filter circuit is fed from full wave rectifier. Generally two capacitors are selected equal.
- The rectifier output is given to the capacitor C_1. This capacitor offers very low reactance to the ac component but blocks dc component.
- Hence capacitor C_1 bypasses most of the ac component. The dc component then reaches to the choke L.
- The choke L offers very high reactance to dc. So it blocks ac component and does not allow it to reach to load while it allows dc component to pass through it.
- The capacitor C_2 now allows to pass remaining ac component and almost pure dc component reaches to the load.
- The circuit looks like a л, hence called л-Filter.

The output voltage is given by

$$V_{DC} = V_m - \frac{V_r}{2} - I_{DC}R_X$$

where V_r = peak to peak ripple voltage

R_X = DC resistance of choke

$$\text{Now } V_r = \frac{I_{DC}}{2fc} \quad \text{for full wave}$$

$$\text{Ripple factor } \gamma = \frac{\sqrt{2}\, X_{C1}X_{c2}}{X_L R_L} = \frac{\sqrt{2}\left(\frac{1}{2\omega C_1}\right)\left(\frac{1}{2\omega C_2}\right)}{(2\omega L)R_L}$$

$$\gamma = \frac{\sqrt{2}}{8\omega^3 L C_1 C_2 R_L}$$

if C_1 & C_2 are expressed in μF and frequency f is assumed to be 50Hz, then we get

$$\gamma \approx \frac{5700}{LC_1C_2R_L}$$

11. why do we need filters in a power supply, under what condition we shall prefer a capacitor filter?

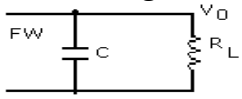
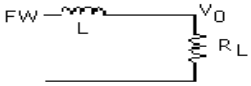
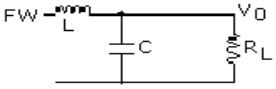
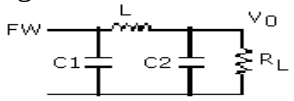
Ans: The circuit which can be used to minimize the undesirable A.C in the output of a rectifier and leaving only the DC component to appear at the output is known as filter. In power supplies, the output of rectifier contains both AC and DC components. Thus, filters are used to remove unwanted ripple contents from this pulsating DC to get pure DC voltage. Even though, the output of a filter is not exactly a constant DC level. Thus, the output of a filter must be fed to a regulator which gives steady DC output.

The capacitive filter is an inexpensive filter for light loads which is connected directly across the load. The main function of capacitor is to allow AC component and block the DC component. Even though, it is a simple circuit to obtain pure DC voltage, but is inefficient due to the following reasons,

- The ripple factor is dependent on the load resistance , R_L.
- The output obtained using capacitor filter is not smooth as desired.
- The values of capacitor or load resistance must be fairly large to obtain a ripple voltage triangular waveform.

12. Compare all the filter circuits from the point of view of ripple factor.

Ans.

Capacitor Filter	**Inductor Filter**	**L – section or LC Filter**	**CLC or л Filter**
1.The circuit arrangement for capacitor filter is shown in figure. 	1.The circuit arrangement for Inductor filter is shown in figure. 	1.The circuit arrangement for L-section filter is shown in figure. 	1.The circuit arrangement for CLC filter is shown in figure. 
2. The expression for ripple factor is, $\gamma = \frac{1}{4\sqrt{3}f_C R_L}$ for FWR	2. The expression for ripple factor is, $\gamma = \frac{R_L}{3\sqrt{2}\omega L}$	2. The expression for ripple factor is, $\gamma = \frac{1}{6\sqrt{2}\omega^2 LC}$	2. The expression for ripple factor is, $\gamma = \frac{\sqrt{2}}{8\omega^2 LC_1C_2R_L}$
3. This filter is operated at large values of C and R_L because the ripple factor is very small at these values.	3. This filter is operated at small values of R_L because it gives a very less ripple factor and requires very high values of L (for less ripple factor) which increases the cost.	3. This filter does not depend on the value of load resistance R_L, it only depends on L and C values which are preferred to be high values for low RF.	3. This filter depends on load resistance R_L. This filter is generally preferred to operate at very high values of L, C_1 & C_2 . R_L for small RF value.
4. The ripple voltage depends on load current i.e., load resistance resistance.	4. The ripple voltage depends on load current.	4. The ripple voltage is independent of the load current.	4. The ripple voltage depends on load current i.e., load resistance.

Problem1.

An a.c. supply of 230V is applied to a half-wave rectifier circuit through transformer of turns ration 5:1. Assume the diode is an ideal one. The load resistance is 300Ω.
Find (a) dc output voltage (b) PIV (c) maximum value of load current (d) average value of load current and (e)power delivered to the load.

Sol:

a) The transformer secondary voltage = 230/5 = 46V.

Maximum value of secondary voltage, $V_m = \sqrt{2}$ x 46 = 65V.

dc voltage = $V_{DC} = \frac{V_m}{л} = \frac{65}{\pi} = 20.7V$

b) PIV of a diode = V_m = 65V

c) Maximum value of load current $I_m = \frac{V_m}{R_L} = \frac{65}{300} = 0.217A$

Therefore, maximum value of power delivered to the load

$$P_m = I_m^2 \times R_L = (0.217)^2 \times 300 = 14.1W$$

d) The value of load current $I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.7}{300} = 0.069A$

e) Therefore average power delivered to the load $P_{dc} = I_{dc}^2 \times R_L = (0.069)^2 \times 300 = 1.43W$

Problem2.

A Full-wave rectifier circuit uses two silicon diodes with a forward resistance of 20Ω each. A dc voltmeter connected across the load of 1kΩ reads 55.4volts. Calculate

i) I_{RMS},
ii) Average voltage across each diode,
iii) Ripple factor, and
iv) Transformer secondary voltage rating.

Sol:

Given R_f = 20Ω, R_L= 1KΩ, V_{dc} = 55.4V

For a FWR $V_{DC} = \frac{2V_m}{л}$ $\therefore V_m = \frac{55.4 \times \pi}{2} = 86.9V$

$$I_m = \frac{V_m}{R_f + R_L} = 0.08519A$$

i) $I_{rms} = \frac{I_m}{\sqrt{2}} = 0.06024A$

ii) $V = \frac{86.9}{2} = 43.45V$

iii) Ripple factor = $\gamma = \sqrt{\left[\frac{I_{rms}}{I_{dc}}\right]^2 - 1}$

$I_{DC} = \frac{2I_m}{л} = 0.05423A$

$I_{rms} = \frac{I_m}{\sqrt{2}} = 0.06024A$

$\gamma = 0.48$

iv) Transformer secondary voltage rating

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{86.9}{\sqrt{2}} = 61.49V$$

Problem3.

A 230V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in the Full-wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together has a resistance of 100Ω.

Determine:

i) dc voltage across the load,

ii) dc current flowing through the load,
iii) dc power delivered to the load, and
iv) ripple voltage and its frequency.

Sol: Given $V_{p(rms)} = 230V$

$$\frac{N_2}{N_1} = \frac{2V_{s(rms)}}{V_{p(rms)}}$$

$$\frac{1}{5} = \frac{2V_{s(rms)}}{230}$$

$$V_{s(rms)} = 23V(each\ half)$$

Given $R_L = 900\Omega, \quad R_f + R_s = 100\Omega$

$$I_m = \frac{V_m}{R_f+R_s+R_L} = \frac{\sqrt{2}\,V_{s(rms)}}{R_f+R_s+R_L} = \frac{\sqrt{2}\times 23}{900+100} = 0.03252A$$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2\times 0.03252}{\pi} = 0.0207A$$

i) $V_{dc} = \frac{2V_m}{\pi} = 20.7V$

ii) $I_{dc} = 0.0207V$

iii) $P_{dc} = V_{dc}I_{dc} = 0.4W$

iv) $PIV = 2V_m = 65.0538V$

v) $Ripple\ factor = \frac{V_{r(rms)}}{V_{dc}} = 0.482$

$$Ripple\ Voltage = V_{r(rms)} = 0.482 \times 20.7 = 9.97V$$

Frequency of ripple=2f =2×60 = 120 Hz.

Problem4.
In a bridge rectifier the transformer is connected to 220V, 60Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diode to be ideal, find:
i) Idc
ii) voltage across the load
iii) PIV assume load resistance to be 1kΩ

Sol: $\frac{N_2}{N_1} = \frac{1}{11} = \frac{V_{s(rms)}}{220}$

$$V_{s(rms)} = \frac{220}{11} = 20V$$

$$V_m = \sqrt{2}\ V_{s(rms)} = 28.2842V$$

i) $I_m = \frac{V_m}{R_L} = \frac{28.2842}{1\times 10^3} = 28.2842mA$

$$\therefore I_{dc} = \frac{2I_m}{\pi} = 18mA$$

ii) $V_{dc} = I_{dc}R_L = 18 \times 10^{-3} \times 1 \times 10^3 = 18V$

iii) $PIV = V_m = 28.2842V$

Problem5.

A 15-0-15 V (rms) ideal transformer is used with a full wave rectifier circuit with diodes having forward drop of 1V. The load is a resistance of 100Ω and a capacitor of 10000μF is used as a filter across the load resistance. Calculate the dc load current and the voltage.

Sol: $V_m = \sqrt{2}\, V_{s(rms)} = \sqrt{2} \times 15 = 21.2132V$

$R_L = 100\Omega, \quad diode\ drop = V_D = 1V, \quad C = 10000\mu F.$

$I_m = \frac{V_m - V_D}{R_L} = \frac{21.2132 - 1}{100} = 0.20213A$

$\therefore I_{rms} = \sqrt{2}\, I_m = 0.2858A$

$\therefore I_{dc} = \frac{2I_m}{\pi} = 0.1286A$

$V_{dc} = V_m - I_{dc}\left[\frac{1}{4fc}\right] - V_D = 20.1489V$

Problem6.

In a FWR circuit using an LC filter, L=10H, C=100μF and R_L=500Ω. Calculate I_{dc} , V_{dc} , ripple factor for an input of $v_i = 30\sin(100\pi t)V$.

Sol: $v_i = V_m \sin \omega t$

$V_{sm} = V_m = 30\ V$

$V_{dc} = \frac{2V_m}{\pi} = \frac{2\times 30}{\pi} = 19.0985V$

$I_{dc} = \frac{V_{dc}}{R_L} = \frac{19.0985}{500} = 38.19mA$

Ripple factor $\gamma = \frac{1}{6\sqrt{2}\omega^2 LC}$ $\quad where\ \omega = 100\pi$

$\gamma = 1.194 \times 10^{-3}$

13 How Zener diode works as a voltage regulator.

Zener Diode Regulator

In a regulator using zener diode, the zener diode is operated in the breakdown condition where the voltage across zener is nearly constant, inspite of the changes in the zener current. So it can be used to regulate the voltage with varying input voltage or varying load conditions.

3.18.1 Regulation with a Varying Input Voltage

The Fig. 3.55 shows how a zener diode can be used to regulate a varying input voltage, commonly known as line regulation. As the input voltage varies, I_Z also varies accordingly. But the zener diode maintains constant voltage across the output terminals over the certain range. These limitations on the input variations are set by the minimum and maximum current values with which the zener can operate.

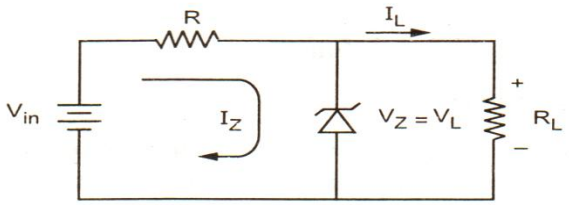


Fig. 3.55 Zener regulation of a variable input voltage

For example, if $I_{Z\ min}$ = 5 mA, $I_{Z\ max}$ = 50 mA, V_Z = 6.8 V and the current limiting sistance R is 1 kΩ then

For minimum current,

Voltage across R = (V_R) = 5 mA × 1 kΩ = 5 V

Since $V_R = V_{IN} - V_Z$ then

3.18.2 Regulation with a Varying Load

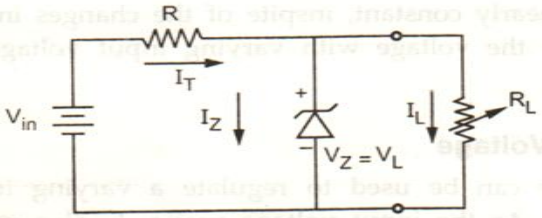


Fig. 3.56 Zener regulator with variable load

The Fig. 3.56 shows a zener regulator with a variable load resistance. This is also referred to as load regulation.

The zener diode maintains a constant voltage across R_L as long as the zener current is greater than $I_{Z\ min}$ and less than $I_{Z\ max}$. When the load current varies, the zener diode current adjusts itself so that its terminal voltage remains constant. For example, if $I_{Z\ min}$ = 5 mA, $I_{Z\ max}$ = 50 mA, V_Z = 10 and V_{in} = 20 V then at no load $R_L = \infty$ and I_L = 0.

Therefore to limit maximum current to 50 mA (I_{Zmax})

$$R_{(min)} = \frac{V_{in} - V_Z}{I_{Z\ max}} = \frac{20V - 10V}{50mA}$$

$$= 200\ \Omega$$

As you know I_Z min = 5 mA, the maximum load current is 45 mA (50 – 5). This shows that the zener diode in this circuit can maintain output voltage constant for load current from 0 mA to 45 mA.

14.Write short notes on shunt and series voltage regulator

3.17.1 Shunt Voltage Regulator

The heart of any voltage regulator circuit is a control element. If such a control element is connected in shunt with the load, the regulator circuit is called shunt voltage regulator. The Fig. 3.54 (a) shows the block diagram of shunt voltage regulator circuit.

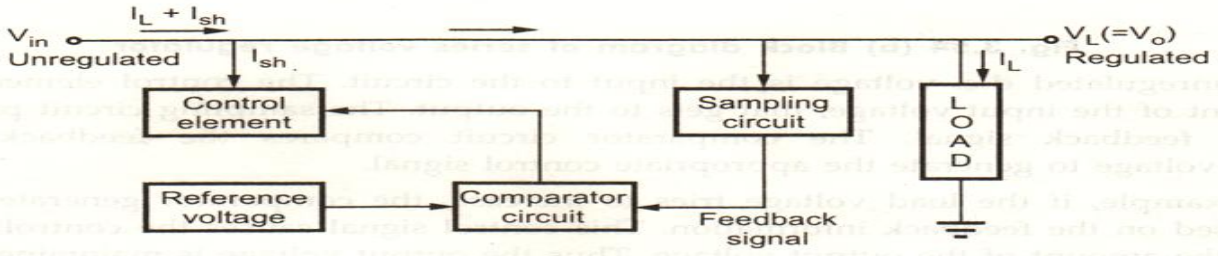


Fig. 3.54 (a) Block diagram of shunt voltage regulator

The unregulated input voltage V_{in}, tries to provide the load current. But part of the current is taken by the control element, to maintain the constant voltage across the load. If there is any change in the load voltage, the sampling circuit provides a feedback signal to the comparator circuit. The comparator circuit compares the feedback signal with the reference voltage and generates a control signal which decides the amount of current required to be shunted to keep the load voltage constant. For example, if load voltage increases then comparator circuit decides the control signal based on the feedback information, which draws increased shunt current I_{sh} value. Due to this, the load current I_L decreases and hence the load voltage decreases to its normal. Thus control element maintains the constant output voltage by shunting the current, hence the regulator circuit is called voltage shunt regulator circuit.

As seen from the block diagram, only part of the load current required to be diverted, passes through the control element. Thus the control element is low current, high voltage rating component. The efficiency depends on the load current I_L. Hence shunt regulators are not preferred for varying load conditions.

3.17.2 Series Voltage Regulator

If in a voltage regulator circuit, the control element is connected in series with the load, the circuit is called series voltage regulator circuit. The Fig. 3.54 (b) shows the block diagram of series voltage regulator circuit.

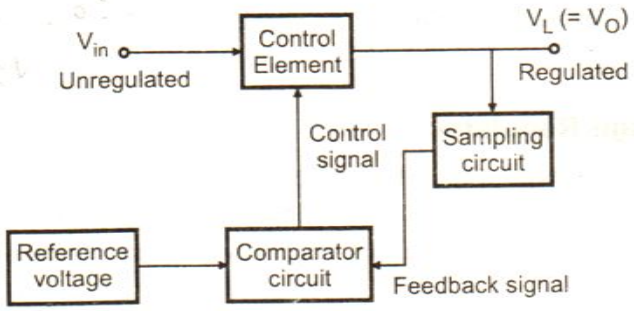


Fig. 3.54 (b) Block diagram of series voltage regulator

The unregulated d.c. voltage is the input to the circuit. The control element, controls the amount of the input voltage, that gets to the output. The sampling circuit provides the necessary feedback signal. The comparator circuit compares the feedback with the reference voltage to generate the appropriate control signal.

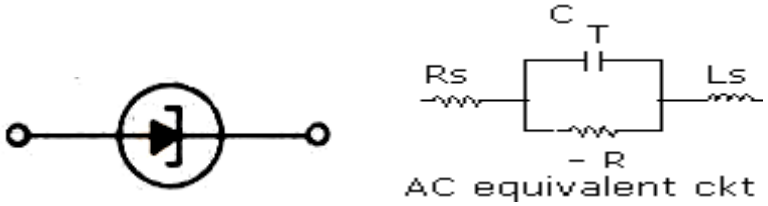
For example, if the load voltage tries to increase, the comparator generates a control signal based on the feedback information. This control signal causes the control element to decrease the amount of the output voltage. Thus the output voltage is maintained constant.

Thus, control element which regulates the load voltage, based on the control signal is in series with the load and hence the circuit is called series voltage regulator circuit.

In series regulators, the entire current passes through the control element and hence control element is high current, low voltage rating component. As input current and load current are same, the efficiency depends on output voltage. It provides good regulation than shunt regulators. It can be used for fixed voltage as well as variable voltage requirements. To compensate for the drop across the control element, input voltage V_{in} must be at least 2 to 3 V more than output voltage.

15. Explain about tunnel diode and V-I characteristics.

A **Tunnel diode**



- A normal pn-junction has an impurity concentration of about 1 part in 10^8 and depletion layer of width 5 micron.
- If the concentration of impurity atoms is greatly increased, say 1 part in 10^3 the device characteristics are completely changed. The new diode was announced in 1958 by Leo Esaki. This diode is called 'Tunnel diode' or 'Esaki diode'.
- As the depletion width decreases there is a large probability that an electron will penetrate through the barrier. This quantum mechanical behavior is referred to as tunneling and hence these high impurity density pn-junction devices are called Tunnel diodes. This phenomenon is called as 'tunneling'.

The volt-ampere characteristic

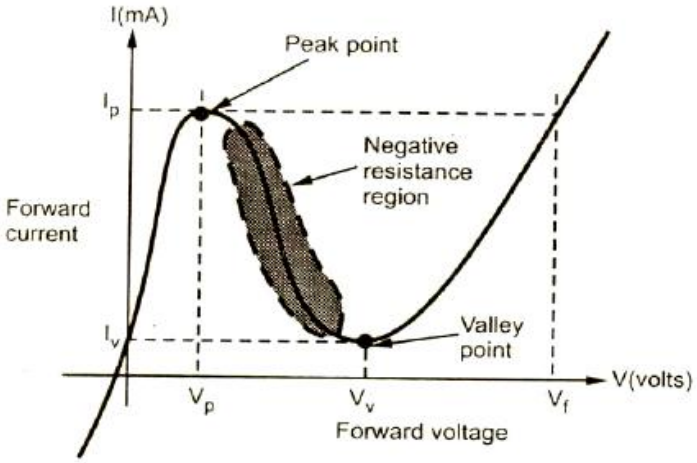


Fig.-I Characteristics of a tunnel diode.

- As soon as the forward bias is applied to the tunnel diode, a significant amount of current is produced. This current immediately reach its peak value.
- The variation of peak current(I_P) is due to narrow depletion region of the junction. So as to voltage increases from 0 to V_P, the current increases from 0 to I_P with the further increase in forward voltage the diode current starts decreasing.
- Thus from peak point to valley point, the current decreases as voltage increases. This results in a negative resistance.
- For voltage greater than V_V, current starts increasing as in case of conventional diode.
- If the tunnel diode is reverse biased, then it acts like a good conductor.

Applications of Tunnel diode:

1. Relaxation oscillator
2. High speed switching networks
3. Micro wave oscillators
4. Amplifiers

16. Explain the principle operation of varactor diode and list out the applications.

Ans

- Also called Varicap, epicap, voltage variable capacitance(VVC), tuning diodes.
- It can be operated under reverse biased condition.
- We know that the transition capacitance c(t) is given by c(t)= εA/W
- As the transition capacitance varies with the applied reverse voltage, it can be used as a voltage Variable capacitance

Operation and characteristics

When a reverse bias is applied to a pn junction, the holes in the p-region move away from the junction and are attracted to the positive terminal and electrons in the n-region move away from the junction and attracted to the negative terminal as shown in Fig.2.56(a). The flow of holes and electrons away from the junction increase depletion layer. The depletion layer is a region with no current carriers and acts as in insulator. The depletion region can be controlled using reverse bias voltage. Since the depletion layer is an insulator, the pn junction can be thought of a parallel plate capacitor, where the p and n regions act like plates of a capacitor.

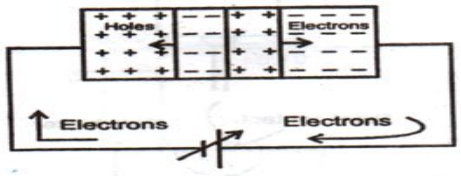


Fig.2.56(a)

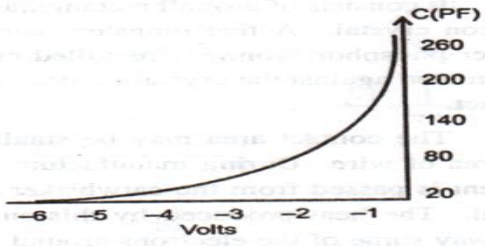


Fig.2.56(b) C-V Characteristics of varactor diode

We know that the depletion region increases as reverse voltage applied to the diode increases. Since capacitance varies inversely as dielectric thickness ($C_T = \frac{\epsilon A}{W}$; As W increases C decrease), the junction capacitance will decrease as the voltage across pn junction increase. That is as reverse voltage across pn junction is varied the capacitance is also varied as shown in Fig.2.56(b).

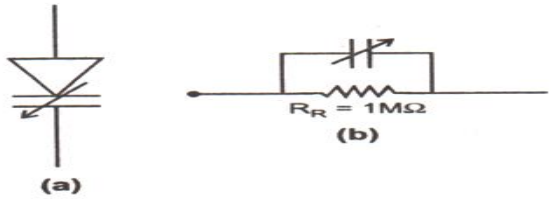


Fig. 2.57 (a) Symbol of varactor diode (b) Equivalent circuit of varactor diode

The symbol and equivalent circuit of varactor diode is shown in Fig.2.57. At low frequencies the capacitance is negligible as the diode appears essentially open because $R_R \rightarrow \infty$. At high frequencies the voltage controlled capacitor has the dominant effect.

Applications

1. **The varactor diode is used in TV receivers, HFC circuit adjustable bandpass filters.**
2. **Used in phase locked loop (PLL) and frequency locked loops (FLL).**
3. **In frequency modulation.**
4. **In high frequency multipliers.**
5. **Very low noise microwave parametric amplifiers.**

17.Explain briefly about LED

2.46.1 Light Emitting Diode (LED)

The light emitting diode, commonly known as LED is a diode that will give off unstable light when it is energized. It works based on electroluminescence. Electroluminescence is a process that changes an electrical input to a light output, the opposite of a photovoltaic effect.

Structure of LEDs

Based on the structure, LEDs are classified as surface emitting LEDs and edge emitting LEDs. The structure of a surface emitting LEDs is shown in Fig.2.77(a). In the surface emitting structure, light radiates perpendicular to the plane of the pn junction. On the other hand, in edge emitting LEDs, the light is confined to a plane and radiates parallel to the junction as shown in Fig.2.77(b).

The symbol of LED is shown in Fig.2.78.

When a diode is forward biased, the free electrons from n-side and holes from p-side move towards the junction. The electrons from n-side cross the junction and fall into holes. That is, recombination takes place. Since the electron falls from a high energy level to lower energy level during the recombination, it radiates energy. If the diode is of type silicon or germanium, then the energy goes off in the form of heat.

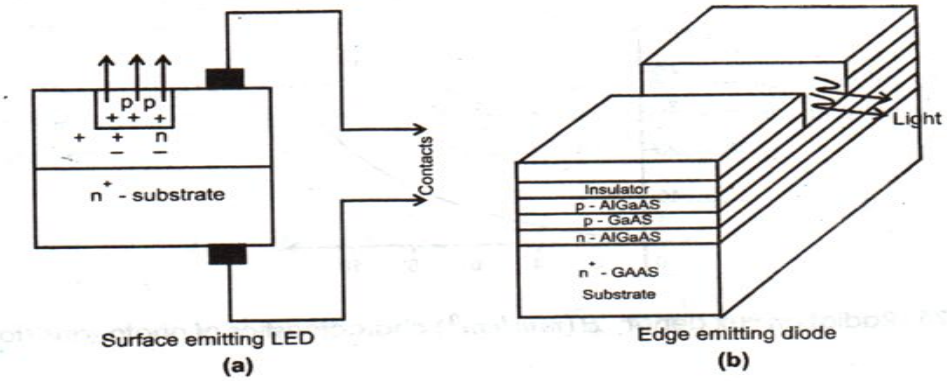


Fig. 2.77 Light emitting diodes

In other materials such as gallium arsenide phosphide (GaAsp) or gallium phosphide (Gap), the energy radiates as light. The colour of the light the LED emits depends on the wave length of the light. Table 2.4 shows the list of components, wavelength and the colour of LEDs.

Table 2.4

Component	Wave length	Colour
Gap	565	Green
GaAsP	590	Yellow
GaAsP	632	Orange
GaAsP	649	Red
GaAlAs	850	Near IR
GaAs	940	Near IR

A number of LEDs can be combined to from an electronic display. One of the most common electronic displays is the seven-segment display shown in Fig.2.79.

Fig. 2.78 Symbol of LED

The seven segment display shown in Fig.2.79 is known as common anode form, since all anodes are connected to a common point. If a positive voltage with respect to ground is connected to the common - anode each individual segment is activated.

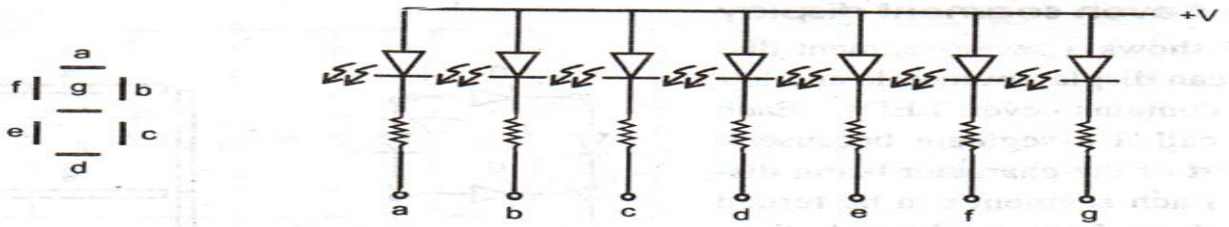


Fig. 2.79 Seven segment display

Applications

1. LEDs are more popularly used in displays clocks, audio and video equipments, traffic lights.
2. It is also used as light source in optical fiber communication.

18. Explain briefly about LCD

2.51 Liquid Crystal Display (LCD)

The Liquid Crystal Display (LCD) is an electronic display device that operates by applying a varying electric voltage to a layer of liquid crystal, thereby inducing changes in its optical properties. LCDs are commonly used in portable electronic games, in digital cameras and camcorders, video injection systems, electronic bill boards and

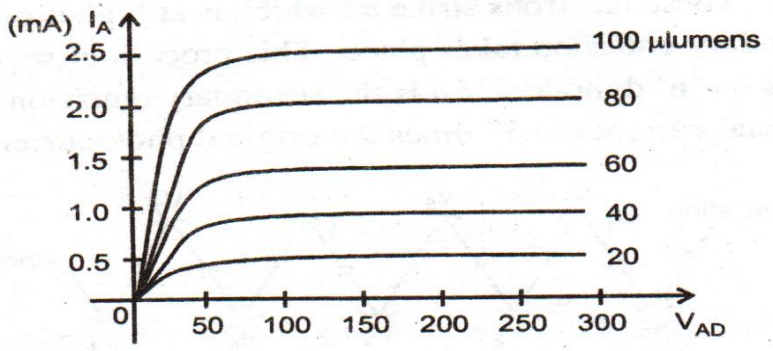


Fig. 2.86 Characteristics of a photo multiplier

monitors for computers. The main advantage of LCD is its low power consumption when compared to that of LED. The power consumption in LCD is in the order of microwatts for the displays as compared to milliwatts in LEDs. To study the operation of LCD, we must know about liquid crystals and their properties.

Liquid crystals

There are three common states of matter that we know: Solid, liquid and gas. Liquid crystal is a fourth state that certain kind of matter can enter into under the right conditions. Solids always maintain their orientation and stay in the same position. The molecules in liquid change their orientation and moves anywhere in the liquid. The molecules in solids exhibit both positional and orientation order. In other words the molecules are constrained to point only certain direction and to be only in certain position with respect to each other. In liquids the molecules do not have position or orientation order, the direction the molecules point and positions are random.

The liquid crystal phase exists between the solid and liquid phase. The molecules tend to maintain their orientation, like the molecules in the solid but also move around

The liquid crystal phase exists between the solid and liquid phase. The molecules tend to maintain their orientation, like the molecules in the solid but also move around

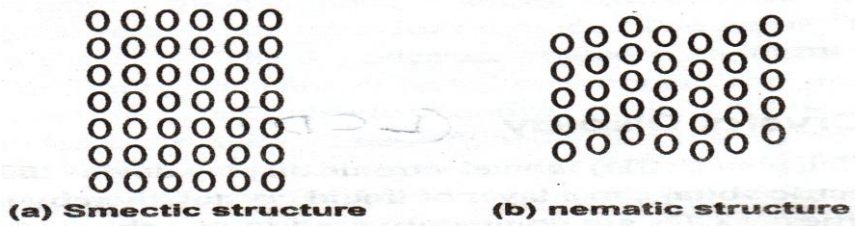


Fig. 2.87 Liquid crystals

to different positions like the molecules in a liquid. The molecules do not point the same direction at all the time. They tend to point more in one direction over time than other directions. The direction is referred to as the director of the liquid crystal.

Liquid crystals are temperature sensitive. It takes fair amount of heat to change in to liquid. They turn in to solid if it is too cold. This phenomenon can, for instance, be observed on laptop screen when it is very hot and very cold.

There are two fundamental ways in which liquid crystals are used to control the properties of light and thereby alter its appearance. They are (i) dynamic scattering method (ii) absorbtion method.

Dynamic scattering method

In dynamic scattering method when an electrical potential is applied, the molecules in the liquid crystal acquire a random orientation. As a result, light passing through the material is reflected in many different directions and a bright, frosty appearance as it emerges.

Absorbtion method

In this method the molecules are oriented in such a way that they alter the polarization of light passing through the material. Polarizing filters are used to absorb or pass the light. Depending on the polarization; it has been given, so light is visible only in those regions where it can energize from the filter.

Each of the above two methods can be operated in two modes.

Transmissive mode

In transmissive mode the LCDs are designed so that light passes completely through them. The light is altered in the desired pattern as it passes through liquid crystal.

Reflective mode

In this mode mirrored surface is used that reflects light back to the viewer. The light is allowed to pass through the material when it is altered and is reflected by a mirror to emerge from the same side it entered.

Dynamic scattering LCD- transmissive mode

Fig.2.88 shows dynamic scattering LCD operated in the transmissive mode. In the region activated by an external electric field, the molecules have random orientation. The molecules in inactivated region have definite alignment. In the activated regions, due to random orientation of molecules the light will be scattered and it escape with a bright appearance.

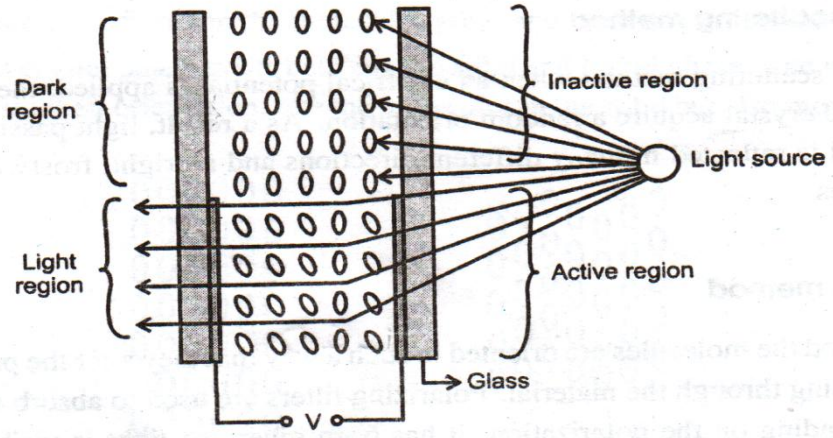


Fig. 2.88 Dynamic scattering LCD; transmissive mode

Dynamic scattering LCD- reflective mode

The construction of dynamic scattering LCD operated in reflective mode is same as that of transmissive type except that a mirrored surface replaced or is added behind one of the glass sheets. However, unwanted reflections limit the readability of display of this type.

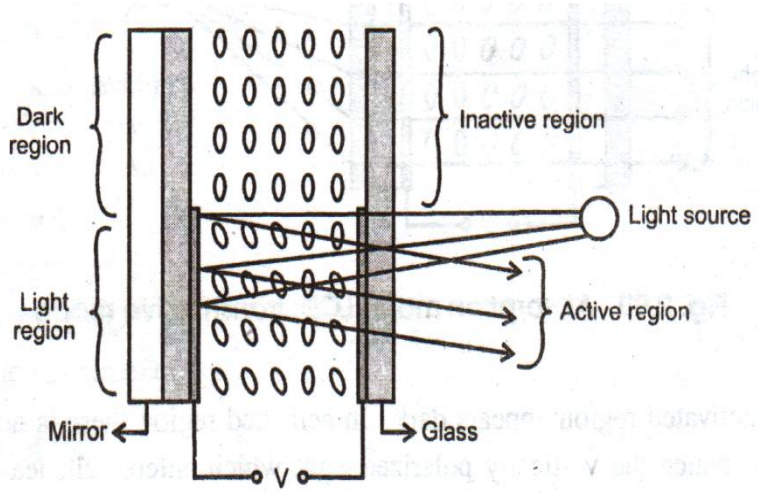


Fig. 2.89 Dynamic scattering LCD; reflective mode

Applications of LCD

LCDs are normally used in

1. Watches
2. Calculators
3. Laptop computers
4. Higher end CROs
5. Portable instrumentation

Comparison between LED and LCD

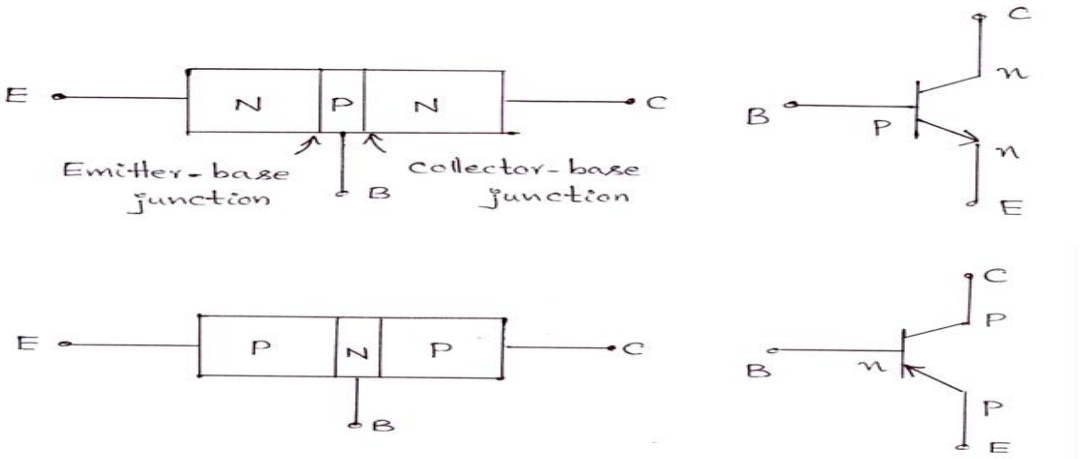
S.No	LED	LCD
1.	Consumes more power.	Consumes less power.
2	Response time is high in the order of 100 nsec.	Response time is less in thc order of 100 to 300 msec.
3	External circuitry is required when driven from ICs.	can be driven directly from ICs.
4	Life time is more.	Life time is limited to 10,000 + hours.
5	Available in red, orange, yellow, green.	Depending on the source of illumination greater range of colour choice.

BIPOLAR JUNCTION TRANSISTOR

1 Define a Transistor. Why transistor is considered as current control device? Explain.

Ans:

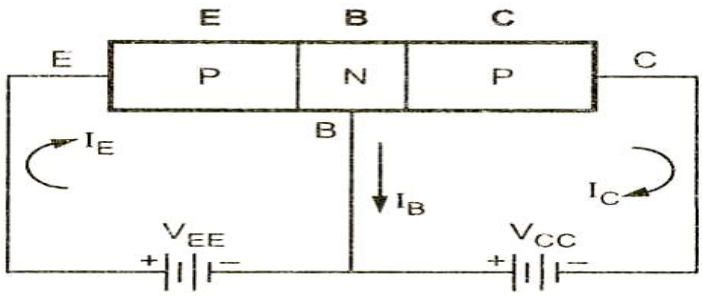
- Transistor means Transfer Resistor i.e., signals are transferred from low resistance circuit into high resistance circuit.
- It is a three terminal semiconductor device : Base, Emitter & Collector.
- It can be operated in three configurations: CB, CE & CC. According to configuration it can be used for voltage as well as current amplification.
- Basically, it is referred as Bipolar Junction Transistor (BJT), because the operation of transistor depends on the interaction of both majority and minority carriers.
- A BJT is formed by placing a P-type silicon layer in between two n-type semiconducting materials or by placing a n-type silicon layer in between two p-type semiconducting materials.



- The emitter terminal is heavily doped so that a large number of charge carriers are injected into the base.
- The base is very lightly doped and is very thin. It allows most of the charge carriers from emitter region to the collector region.
- The collector is moderately doped. Its main function is to collect the majority charge carriers coming from the emitter and passing through the base.

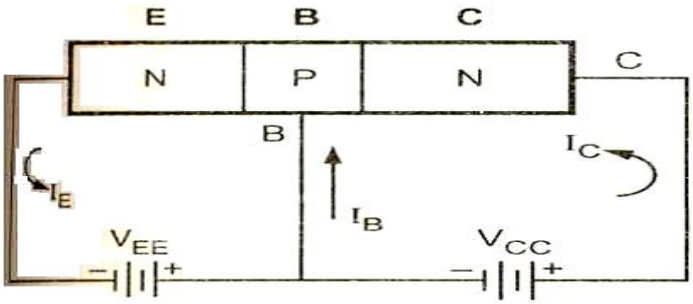
Why transistor is considered as current control device?

- Transistor is also called as current control device, since the output current is controlled by the input current.
- In order to realize such a device, we require a forward biased diode at the input port and a reverse biased diode at the output port.
- Also the reverse current of the output diode must be controlled by the forward current of the input diode.
- Since in the transistor we have two junctions in which one junction is forward biased and other junction is reverse biased.
- The forward biased junction injects holes from the p-side (if it is a PNP transistor) called emitter into the n-region called base which is taken as reference electrode. The reverse biased pn junction produces a minority carrier drift current and the output p-region which collects this current is called the collector.



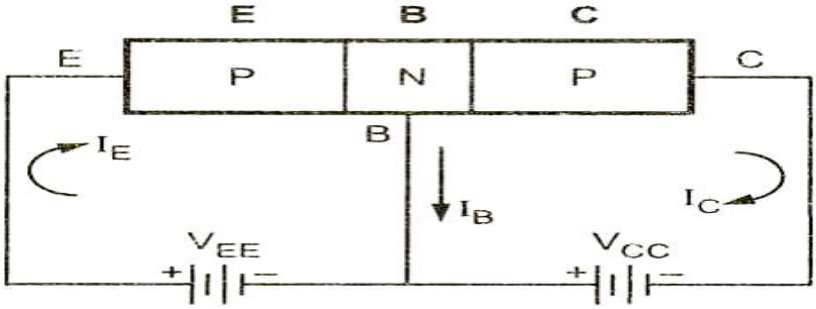
- The emitter current injected into the base increases the minority carrier density in the base and augments the reverse minority carrier drift current flowing in the collector circuit.
- Thus the input emitter current controls the output collector current and the transistor behaves as a current controlled source or simply current control device.

2. With neat diagrams explain the working of npn and pnp transistor.
Ans: Working of a n-p-n transistor:



- The n-p-n transistor with base to emitter junction forward biased and collector base junction reverse biased is as shown in figure.
- As the base to emitter junction is forward biased the majority carriers emitted by the n-type emitter i.e., electrons have a tendency to flow towards the base which constitutes the emitter current I_E.
- As the base is p-type there is chance of recombination of electrons emitted by the emitter with the holes in the p-type base. But as the base is very thin and lightly doped only few electrons emitted by the n-type emitter less than 5% combines with the holes in the p-type base, the remaining more than 95% electrons emitted by the n-type emitter cross over into the collector region constitute the collector current.
  The current distributions are as shown in fig. $\mathbf{I_E = I_B + I_C}$

Working of a p-n-p transistor:



- The p-n-p transistor with base to emitter junction is forward biased and collector to base junction reverse biased is as show in figure.
- As the base to emitter junction is forward biased the majority carriers emitted by the p type emitter i.e., holes have a tendency to flow towards the base which constitutes the emitter current I_E.
- As the base is n-type there is a chance of recombination of holes emitted by the emitter with the electrons in the n-type base. But as the base us very thin and lightly doped only few electrons less than 5% combine with the holes emitted by the p-type emitter, the remaining 95% charge carriers cross over into the collector region to constitute the collector current.
  The current distributions are shown in figure. $\mathbf{I_E = I_B + I_C}$

3. Write short notes on emitter efficiency, Transport factor and large signal current gain.
Ans: Current components in a transistor:

- The figure below shows the various current components which flow across the forward biased emitter junction and reverse-biased collector junction in P-N-P transistor.

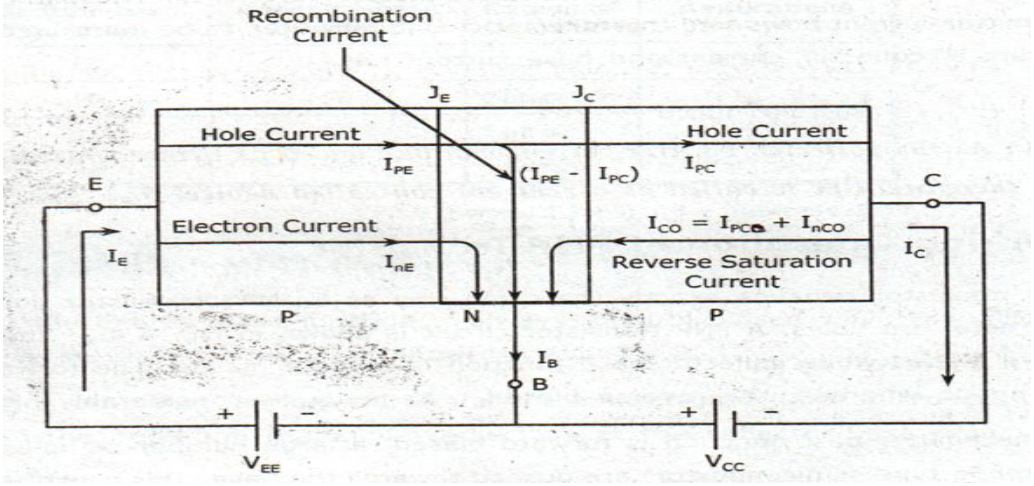


Figure. Current components in a transistor (PNP)

- The emitter current consists of the following two parts:
  1) Hole current I_{pE} constituted by holes (holes crossing from emitter into base).
  2) Electron current I_{nE} constituted by electrons (electrons crossing from base into the emitter).

  Therefore, Total emitter current $I_E = I_{pE}$ (majority)+ I_{nE} (Minority)

- The holes crossing the emitter base junction J_E and reaching the collector base junction J_C constitutes collector current I_{pC}. Not all the holes crossing the emitter base junction J_E reach collector base junction J_C because some of them combine with the electrons in the n-type base.
- Since base width is very small, most of the holes cross the collector base junction J_C and very few recombine, constituting the base current $(I_{pE} - I_{pC})$.
- When the emitter is open-circuited, I_E=0, and hence I_{pC}=0. Under this condition, the base and collector together current I_C equals the reverse saturation current I_{CO}, which consists of the following two parts: I_{PCO} caused by holes moving across J_C from N-region to P-region. In I_{nCO} caused by electrons moving across J_C from P-region to N-region.

1) **Emitter efficiency (γ) :** It is the ratio of current of injected carriers at emitter base junction to total emitter current.

$$\gamma = \frac{\text{current of injected carriers at } J_E}{\text{total emitter current}}$$

In case of pnp transistor, $\gamma = \frac{I_{pE}}{I_{pE}+I_{nE}} = \frac{I_{pE}}{I_E}$

In case of npn transistor, $\gamma = \frac{I_{nE}}{I_{pE}+I_{nE}} = \frac{I_{nE}}{I_E}$

Where, I_{pE} = Injected hole diffusion current at emitter junction.
I_{nE} = Injected electron diffusion current at emitter junction.

2) **Transport factor (β^*) :** It is the ratio of injected carrier current reaching at collector base junction J_C to injected carrier current at emitter base junction J_E.

$$\beta^* = \frac{\text{Injected carrier current reaching } J_C}{\text{Injected carrier current at } J_E}$$

In case of pnp transistor, $\beta^* = \frac{I_{pC}}{I_{pE}}$

In case of pnp transistor, $\beta^* = \frac{I_{nC}}{I_{nE}}$

3) **Large signal current gain(α) :** It is the ratio of the current due to injected carriers I_{pC} to the total emitter current I_E.

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_C - I_{co}}{I_E}$$

$$I_C = \alpha I_E + I_{CO}$$

4) **Relation between α, β & γ:** Multiplying and dividing equation $\alpha = \frac{I_{pC}}{I_E}$ with I_{pE},

$$\alpha = \frac{I_{pC}}{I_{pE}} \times \frac{I_{pE}}{I_E}$$

$$\alpha = \beta^* \gamma$$

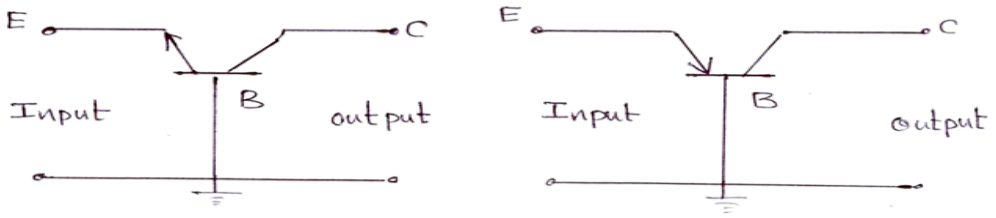
4. What are the different configurations of BJT? Explain.

Ans: Transistor circuit configurations:

- Following are the three types of transistor circuit configurations:
  1) Common-Base (CB)
  2) Common-Emitter (CE)
  3) Common-Collector (CC)
- Here the term 'Common' is used to denote the transistor lead which is common to the input and output circuits. The common terminal is generally grounded.

Common Base (CB) Configuration:

- In this configuration input is applied between emitter and base and output is taken from the collector and base.
- Here, base of the transistor is common to both input and output circuits and hence the name common base configuration.



Here, $I_C = \alpha I_E + I_{CBO}$

Where I_{CBO} is reverse saturation current and it doubles for every 10^0 C rise in temperature. It is negligible small in most practical situations, we can approximately write:

$I_C = \alpha I_E$

$\alpha = \frac{I_C}{I_E}$ this is current amplification factor in CB configuration.

For a transistor, $I_E = I_B + I_C$

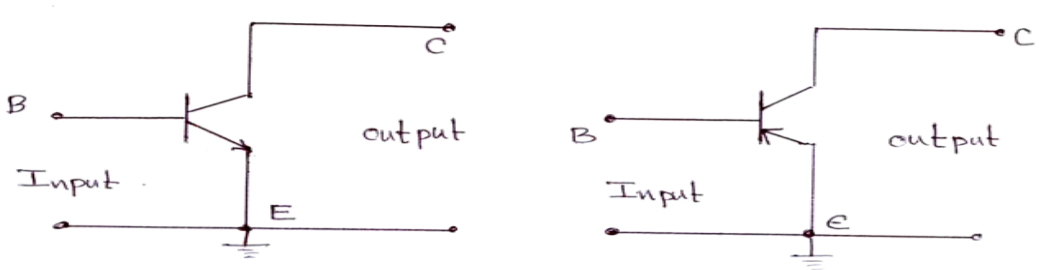
$= I_B + \alpha I_E$

$I_B = I_E - \alpha I_E$

$I_B = I_E[1 - \alpha]$

Common Emitter (CE) Configuration:

- In this configuration input is applied between base and emitter and output is taken from the collector and emitter.
- Here, emitter of the transistor is common to both input and output circuits and hence the name common emitter configuration.



We have seen $I_C = \alpha I_E + I_{CBO}$

$I_C - I_{CBO} = \alpha I_E$

Dividing by α $\frac{I_C}{\alpha} - \frac{I_{CBO}}{\alpha} = I_E$ since $I_E = I_B + I_C$

$$\frac{I_C}{\alpha} - \frac{I_{CBO}}{\alpha} = I_B + I_C$$

$$\frac{I_C}{\alpha} - I_C = I_B + \frac{I_{CBO}}{\alpha}$$

$$I_C\left[\frac{1}{\alpha} - 1\right] = I_B + \frac{I_{CBO}}{\alpha}$$

$$I_C\left[\frac{1-\alpha}{\alpha}\right] = I_B + \frac{I_{CBO}}{\alpha}$$

$$I_C = \left[\frac{\alpha}{1-\alpha}\right] I_B + \left[\frac{1}{1-\alpha}\right] I_{CBO}$$

Now we define new parameter $\beta = \frac{\alpha}{1-\alpha}$

β is always greater than 1

$I_C = \beta I_B + [1+\beta] I_{CBO}$ since $1 + \beta = \frac{1}{1-\alpha}$

The term $[1+\beta] I_{CBO}$ is the reverse leakage current in CE configuration. It is also defined as I_{CEO}

$I_C = \beta I_B + I_{CEO}$

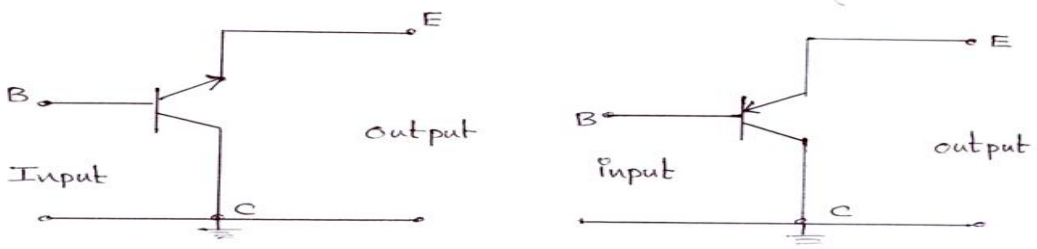
Where I_{CEO} is collector emitter current when base is open. It is neglected in practical circuits.

$I_C = \beta I_B$

$\beta = \frac{I_C}{I_B}$ this is current amplification factor in CE configuration.

Common Collector (CC) Configuration:

- In this configuration input is applied between base and Collector and output is taken from the emitter and collector.
- Here, Collector of the transistor is common to both input and output circuits and hence the name common Collector configuration.



- The current gain of the circuit is defined as the ratio of output current to (I_E) to input current (I_B). It is designated as γ.

$$\gamma = \frac{I_E}{I_B} = \frac{I_E}{I_C} \times \frac{I_C}{I_B} = \frac{1}{\alpha}\beta$$

$$\gamma = \frac{I_E}{I_B} = \frac{\beta}{\alpha} = \frac{\beta}{\frac{\beta}{(1+\beta)}} = (1+\beta)$$

$$\therefore \quad \gamma = \frac{1}{1-\alpha} = 1+\beta$$

It means that output current is (1+β) times the input current.

5. With necessary diagram explain the input and output characteristics of CE configuration.

Ans:

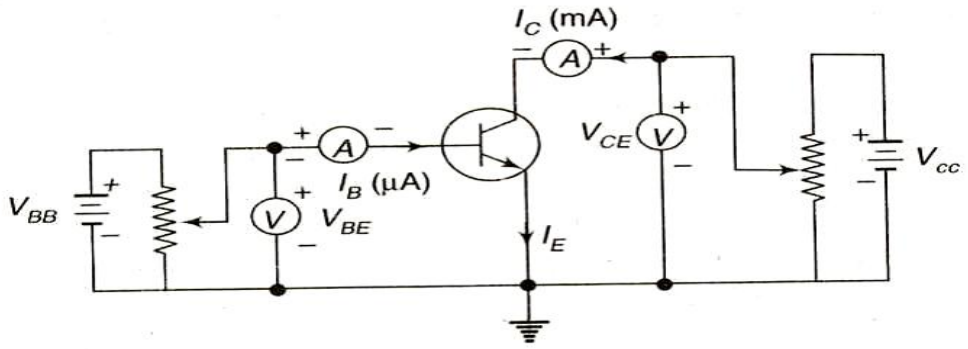


Fig. Circuit to determine CE Static characteristics.

Input Characteristics:

- To determine the input characteristics, the collector to emitter voltage is kept constant at zero volts and base current is increased from zero in equal steps by increasing V_{BE} in the circuit.
- The value of V_{BE} is noted for each setting of I_B. This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B versus V_{BE} are drawn.
- The input characteristics thus obtained are shown in figure below.

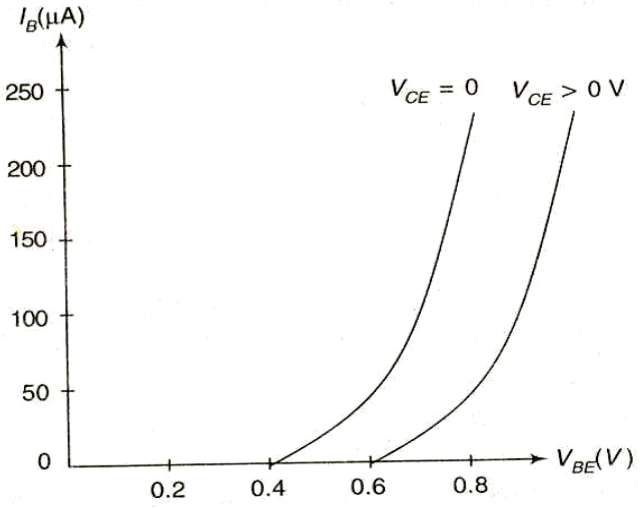


Fig. CE Input Characteristics.

- When V_{CE}=0 , the emitter-base junction is forward biased and the junction behaves as a forward biased diode.
- When V_{CE} is increased, the width of the depletion region at the reverse biased collector-base junction will increase. Hence he effective width of the base will decrease. This effect causes a decrease in the base current I_B. Hence, to get the same value of I_B as that for V_{CE}=0, V_{BE} should be increased. Therefore, the curve shifts to the right as V_{CE} increases.

Output Characteristics:

- To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting base-emitter voltage, V_{BE}. The magnitude of collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting of V_{CE}.
- Now the curves of I_C versus V_{CE} are plotted for different constant values of I_B.
- The output characteristics thus obtained are shown in figure below.

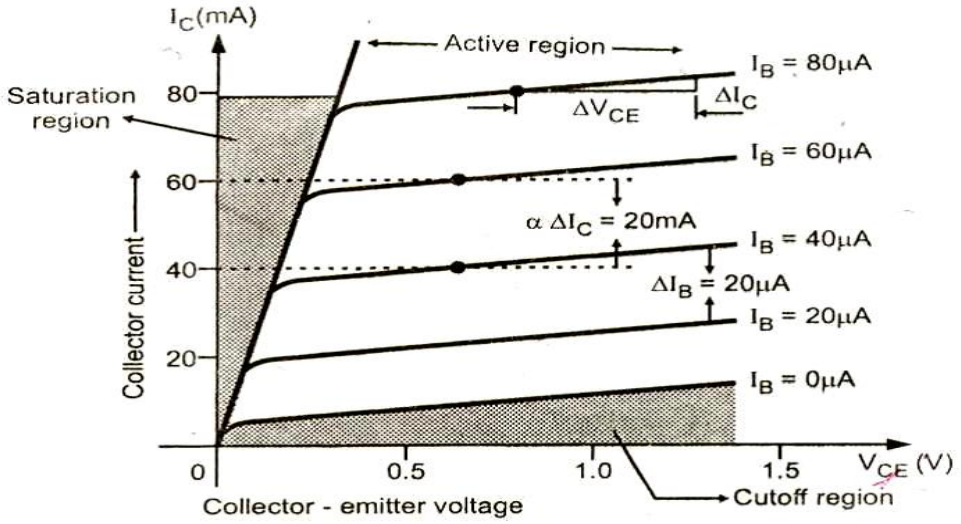


Fig. CE Output characteristics

The output characteristics of common emitter configuration consist of three regions: Active, Saturation and Cut-off regions.

Active Region: The region where the curves are approximately horizontal is the "Active" region of the CE configuration. In the active region, the collector junction is reverse biased. As V_{CE} is increased, reverse bias increase. This causes depletion region to spread more in base than in collector, reducing the changes of recombination in the base. This increase the value of α_{dc} .

This Early effect causes collector current to rise more sharply with increasing V_{CE} in the active region of output characteristics of CE transistor.

Saturation Region: If V_{CE} is reduced to a small value such as 0.2V, then collector-base junction becomes forward biased, since the emitter-base junction is already forward biased by 0.7V. The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region. Thus input characteristics of CE configuration are similar to forward characteristics of p-n junction diode. When both the junctions are forwards biased, the transistor operates in the saturation region, which is indicated on the output characteristics. The saturation value of V_{CE}, designated $V_{CE}(Sat)$, usually ranges between 0.1V to 0.3V.

Cut-Off Region: When the input base current is made equal to zero, the collector current is the reverse leakage current I_{CEO}. Accordingly, in order to cut off the transistor, it is not enough to reduce I_B=0. Instead, it is necessary to reverse bias the emitter junction slightly. We shall define cut off as the condition where the collector current is equal to the reverse saturation current I_{CO} and the emitter current is zero.

6 With necessary diagram explain the input and output characteristics of CB configuration.

Ans:

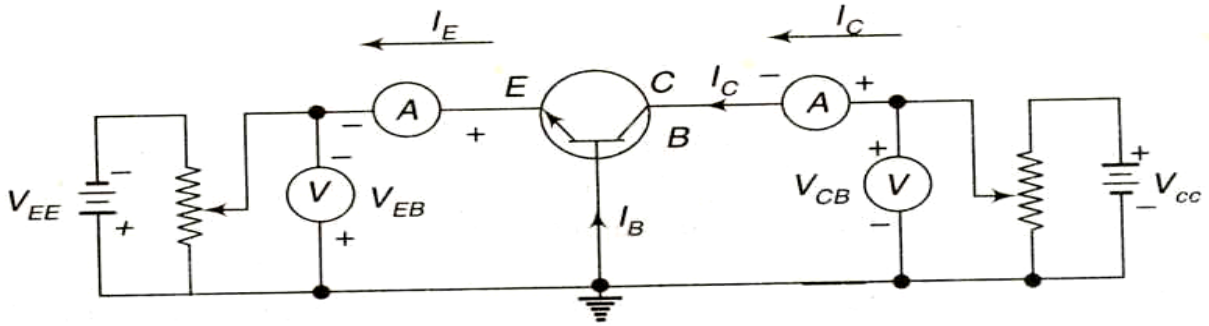


Fig. Circuit to determine CB static characteristics.

Input Characteristics:

To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volts and the emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}.

The input characteristics thus obtained are shown in figure below.

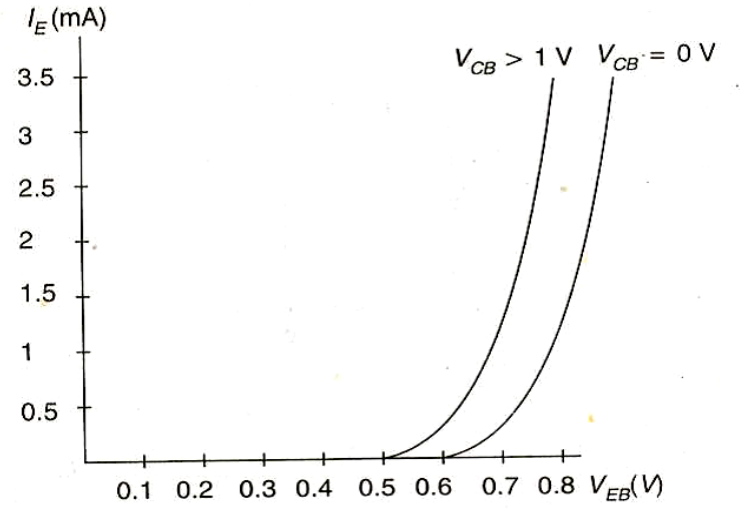
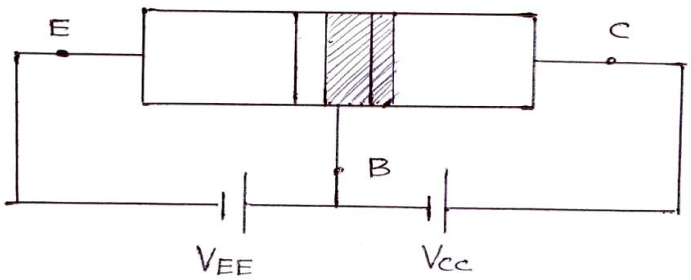


Fig. CB Input characteristics.

Early effect (or) Base – Width modulation:

As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter voltage is known as Early effect (or) Base-Width modulation.



Thus decrease in effective base width has following consequences:

- Due to Early effect, the base width reduces, there is a less chance of recombination of holes with electrons in base region and hence base current I_B decreases.
- As I_B decreases, the collector current I_C increases.
- As base width reduces the emitter current I_E increases for small emitter to base voltage.
- As collector current increases, common base current gain (α) increases.

Punch Through (or) Reach Through:

When reverse bias voltage increases more, the depletion region moves towards emitter junction and effective base width reduces to zero. This causes breakdown in the transistor. This condition is called "Punch Through" condition.

Output Characteristics:

To determine the output characteristics, the emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}. Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of I_E. Now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in figure below.

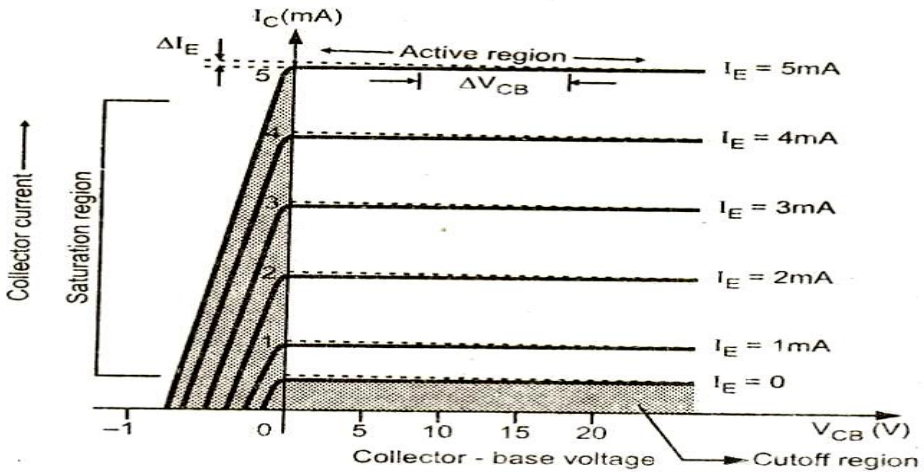


Fig. CB Output characteristics

From the characteristics, it is seen that for a constant value of I_E, I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CB}. Further, I_C flows even when V_{CB} is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e., electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse biased collector-base junction, they flow to the collector region and give rise to I_C even when V_{CB} is equal to zero.

7. With necessary diagram explain the input and output characteristics of CC configuration.

Ans: Characteristics of common collector circuit:

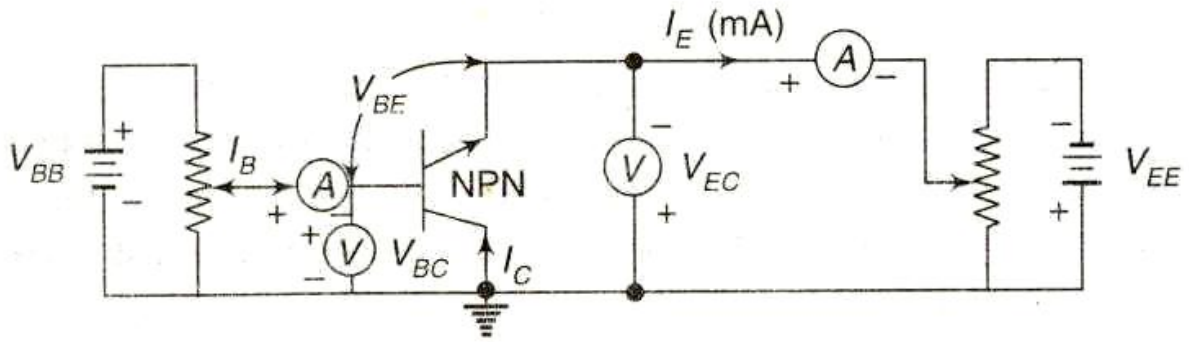


Fig. Circuit to determine CC static characteristics.

Input Characteristics:

To determine the input characteristic, V_{EC} is kept at a suitable fixed value. The base collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. Plots of V_{BC} versus I_B for different values of V_{EC} shown in figure are the input characteristics.

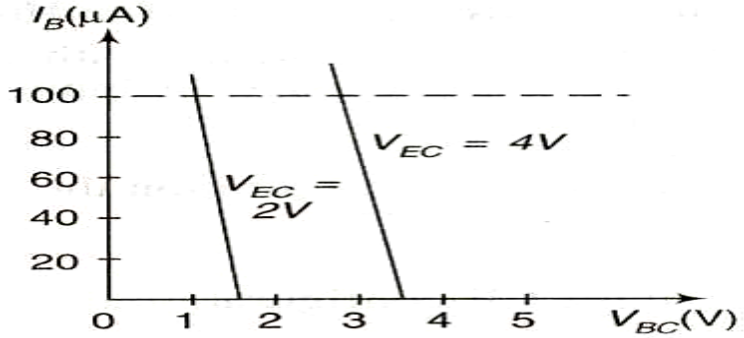


Fig. CC Input Characteristics.

Output Characteristics:

The output characteristics shown in figure below are the same as those of the common emitter configuration.

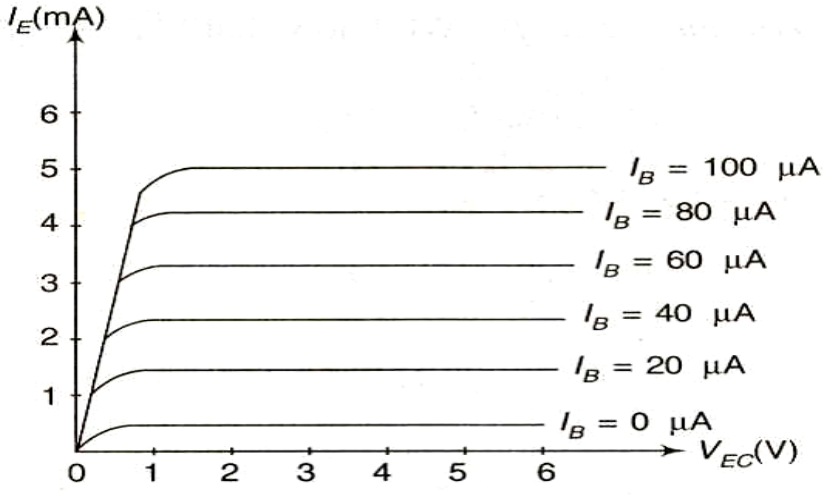


Fig. CC output characteristics.

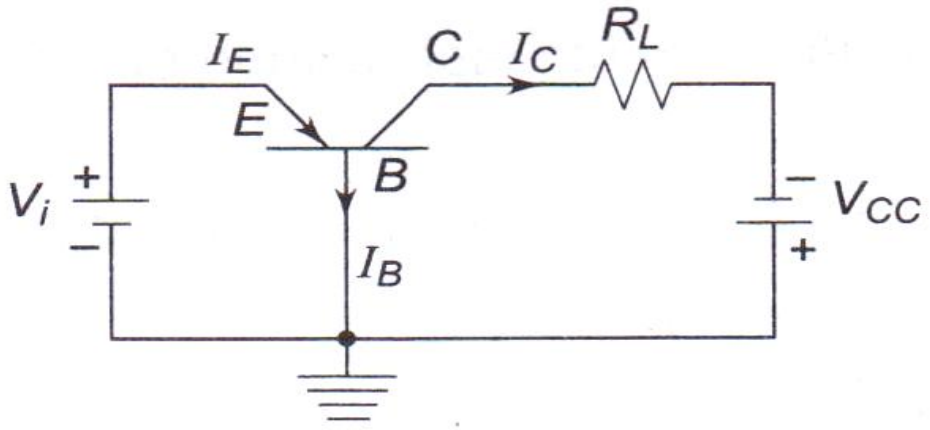
8. Summarize the salient features of the characteristics of BJT operating in CE,CB and CC configurations.

Property	CB	CE	CC
Input Resistance	Low (About 100Ω)	Moderate (About 750Ω)	High (About 750kΩ)
Output Resistance	High (About 450kΩ)	Moderate (About 45kΩ)	Low (About 25Ω)
Current Gain	1	High	High
Voltage Gain	About 150	About 500	Less than 1
Phase Shift between input and output voltages	0° (or) 360°	180°	0° (or) 360°
Applications	For high frequency circuits	For Audio frequency circuits	For impedance matching

9. How Transistor acts as an amplifier

Ans.

- A load resistor R_L is connected in series with the collector supply voltage V_{CC} of CB transistor configuration as shown in figure.



CB transistor configuration

- A small change in the input voltage between emitter and base, say ΔV_i , causes a relatively larger change in emitter current, say ΔI_E.
- A fraction of this change in current is collected and passed through R_L and is denoted by symbol α'.
- Therefore the corresponding change in voltage across the load resistor R_L due to this current is $\Delta V_0 = \alpha' R_L \, \Delta I_E$
- Here , the voltage amplification $A_v = \frac{\Delta V_0}{\Delta V_i}$ is greater than unity and thus the transistor acts as an amplifier.

10. Define α_{dc} , β_{dc} and γ_{dc} of a transistor. Derive the relation among them and write any two applications of transistor.

Ans: α_{dc} : The relation between I_E and I_C due to majority carriers is related by α, in a DC mode. α_{dc} is defined by the following formula,

$$\alpha_{dc} = \frac{I_C}{I_E}$$

β_{dc}: The relation between collector current I_C and base current I_B in a DC mode is defined as, $\beta_{dc} = \frac{I_C}{I_B}$

γ_{dc}: The relation between Emitter current I_E and base current I_B in a DC mode is defined as,

$$\gamma_{dc} = \frac{I_E}{I_B}$$

Relation between α & β

$\alpha = \frac{I_c}{I_E}$, $\beta = \frac{I_c}{I_B}$

Transistor current equation

$I_E = I_c + I_B$

$I_B = I_E - I_c$

$\beta = \frac{I_c}{I_B}$

$\beta = \frac{I_c}{I_E - I_c}$

dividing above equation with I_E, we get

$$\beta = \frac{\frac{I_c}{I_E}}{\frac{I_E}{I_E} - \frac{I_c}{I_E}}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

above equation is β interms of α

adding both sides with 1 we get

$1 + \beta = \frac{\alpha}{1-\alpha} + 1$

$= \frac{\alpha + 1 - \alpha}{1-\alpha}$

$1 + \beta = \frac{1}{1-\alpha}$

$1 - \alpha = \frac{1}{1+\beta}$

$\alpha = 1 - \frac{1}{1+\beta}$

$= \frac{1+\beta-1}{1+\beta}$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

above equation is α interms of β.

relation b/w α & γ

$\alpha = \frac{I_C}{I_E}$, $\gamma = \frac{I_E}{I_B}$

Transistor current equation

$I_E = I_C + I_B$

$I_B = I_E - I_C$

$\gamma = \frac{I_E}{I_E - I_C}$

dividing with I_E

$$\gamma = \frac{1}{1-\alpha}$$

relation b/w β & γ

$\beta = \frac{\alpha}{1-\alpha}$

adding both sides of β with 1 we get

$1+\beta = \frac{\alpha}{1-\alpha} + 1$

$= \frac{\alpha + 1 - \alpha}{1-\alpha}$

$1+\beta = \frac{1}{1-\alpha}$

$$\gamma = 1+\beta$$

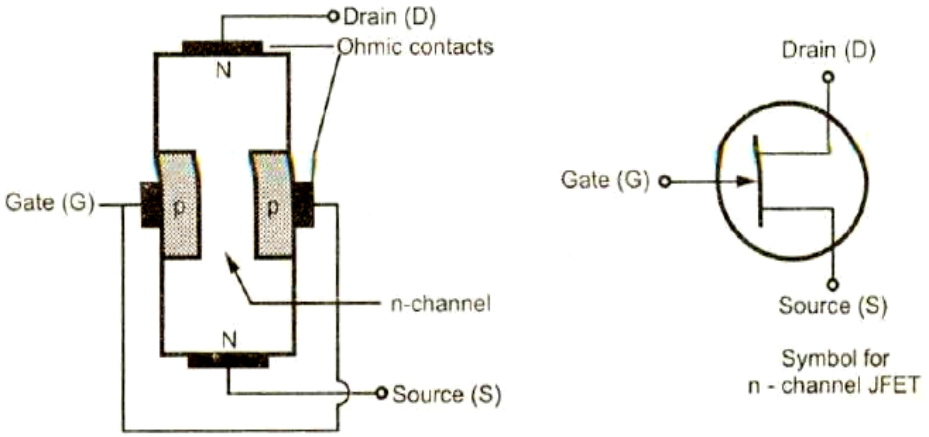
Application of transistor:

- Used in amplifier circuits
- Used in oscillator circuits
- Used as a switch in digital circuits
- It finds many applications in computers, satellites and modern communication systems.

11. Draw the structure of an N- channel JFET and explain its principle of operation with Characteristics.

Ans. Structure and symbol of n-channel JFET:

The structure and symbol of n-channel JFET are shown in figure below

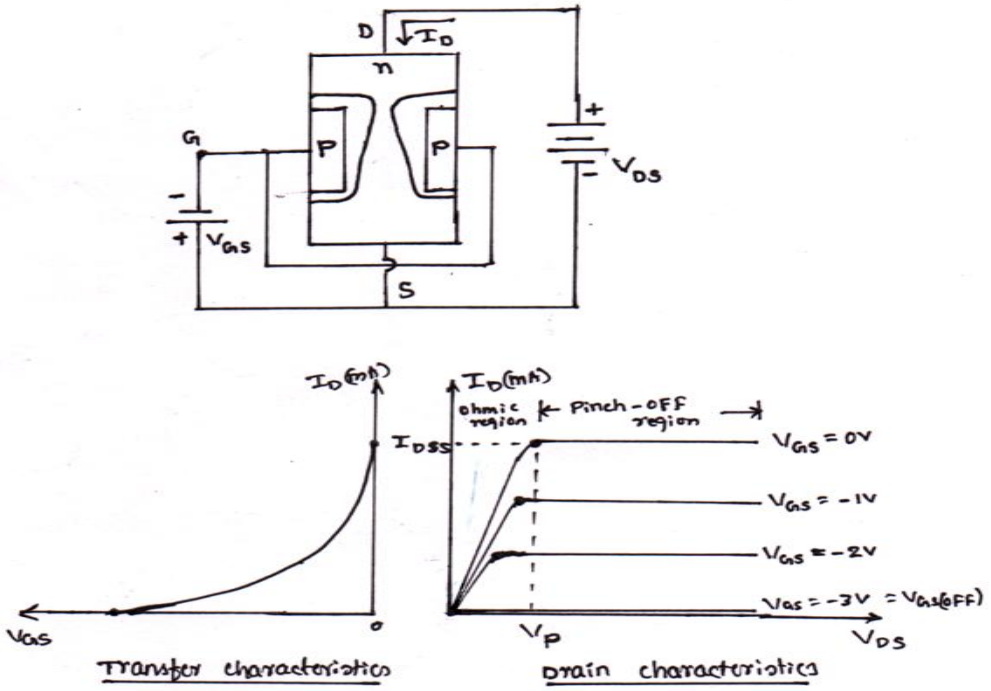


(a) Structure of N- channel JFET (b) Symbol

The electrons enter the channel through the terminal called 'source' and leave through the terminal called 'drain'. The terminals taken out from heavily doped electrodes of p-type material are called 'gates'. Usually, these electrodes are connected together and only one terminal is taken out, which is called 'gate.

Operation of N-Channel JFET:

When V_{GS}=0 and V_{DS} =0: In this case the drain current $I_D = 0$.



When V_{GS}=0 and V_{DS} is increased from zero: The instant V_{DS} is applied the electrons starts flowing from source drain terminal, establishing the current I_D. The current I_D flowing through the channel causes a voltage drop between drain and source. The depletion region is wider near the top of P material when compared to bottom P region. As V_{DS} is increased there is further increase in the reverse bias applied to top of P type material which further increases the width of the depletion region. At some V_{DS} the depletion regions from two sides of the channel eventually meet that is channel is said to be pinched off and the drain voltage is called the *pinch off voltage* V_P. However in reality a very small channel still exist, with a current of very high density and I_D maintains a saturation level. At this point I_D is referred to as drain source saturation current I_{DSS}.

When V_{DS}=0 and V_{GS} is decreased from zero(- ve)

As V_{GS} is decreased from zero, the reverse bias voltage across the P-N junction is increased and hence, the thickness of the depletion region in the channel increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cut-off.

12. Why FET is called unipolar device and is called as voltage operated device? What are the important characteristics of FET?

Ans. A device in which the flow of current through the conducting region is controlled by an electric field is called as FET. The conduction current flows only due to majority carriers. Thus, FET is called as unipolar device.

FET is also called as voltage controlled device because the voltage at the input terminal controls the output current.

Important characteristics of FET

- The flow of current in the conduction region is only due to majority carriers.
- The conduction is through an N-type or p-type semiconductor material due to the absence of junctions.
- FET has very high input impedance of the order 100MΩ.
- FET has lower output impedance.
- FET is a voltage controlled device.
- FET amplifiers have low gain bandwidth product due to the junction capacitive effects.
- FET has higher switching speeds and cut-off frequencies.
- FET has negative temperature coefficient at high current levels.

13. why we call FET as a voltage controlled device?

Ans: For a Junction Field Effect Transistor under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and behave as an almost pure ohmic resistor. Maximum drain-source current I_{DSS} and minimum resistance will exist when the gate-source voltage is equal to zero volts (i.e., $V_{GS}=0$). If the gate voltage is increased (i.e., negatively for N-channel JFETs and positively for P-channel JFETs), the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is represented as $V_{GS}=V_{GS(OFF)}$.

By changing the voltage applied on the FET's gate pin, the resistance offered by the FET's channel changes and different currents are drawn from the circuit for different values of resistance. Thus, the load current (drain-source current) of a FET is controlled by the voltage applied on the gate pin. Hence, FETs are acts as voltage controlled device.

14. Define JFET Parameters

i) DC drain resistance
ii) AC drain resistance
iii) Transconductance
iv) Amplification factor

Ans: i) DC drain resistance, r_d

It is defined as the ratio of drain to source voltage to drain current by keeping the gate to source voltage constant. The DC drain resistance is given by

$$R_D = \frac{V_{DS}}{I_D}\Big|_{V_{Gs}=Constant}$$

ii) AC drain resistance, r_d

It is defined as the ratio of change in drain to source voltage to the change in drain current at a constant gate to source voltage.

$$r_D = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{Gs}=Constant}$$

iii) Transconductance, g_m

It is defined as the rate of change of drain current with change in gate to source voltage by keeping the drain to source voltage constant. It is denoted by 'g_m'.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}=Constant}$$

Its units are ampere per volt or mS (milli Siemen). It is also called as mutual conductance.

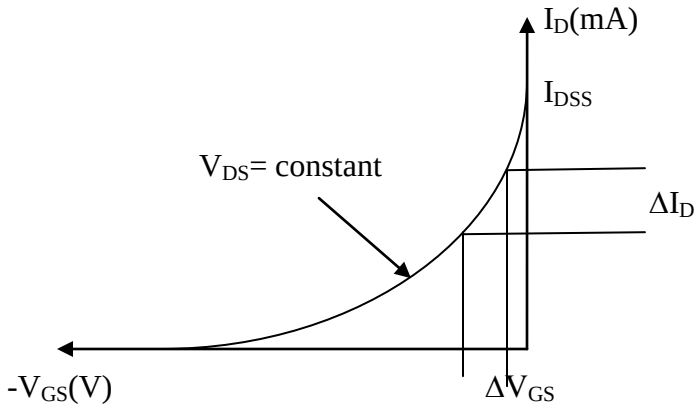


Fig. Transfer characteristics

Figure shows the graph of I_D versus V_{GS}, from this a relation for g_m can be deduced as,

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_p}\right]$$

Where g_{mo} = value of g_m at V_{GS}= 0, is $\frac{-2I_{DSS}}{V_p}$

V_p = Pinchoff voltage.

IV) Amplification Factor, μ

It is defined as the ratio of change in drain to source voltage to change in gate to source voltage keeping the drain current constant.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D = Constant}$$

The above expression can also be written as,

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = r_D \times g_m$$

15. What are the differences between BJT and FET?

Ans.

- FET is a unipolar device, where as BJT is a bipolar device.
- FET is a voltage controlled device where as, BJT is a current controlled device.
- FET has high input resistance than BJT.
- FET is less noisy than BJT.
- FETs are more thermal stable than BJT.
- FET is less affected by radiation.
- FETs are much easier to fabricate than BJT.
- FET has small size, high efficiency and longer life.

16. Compare N-channel with P-Channel FET's and What are the applications of JFET?

Ans:

1. In an N-channel JFET the current carriers are electrons, whereas the current carriers are holes in a P-channel JFET.
2. Mobility of electrons is large in N-channel JFET, mobility of holes is poor in P-channel JFET.
3. The input noise is less in N-channel JFET than that of P-channel JFET.
4. The transconductance is larger in N-channel JFET than that of P-channel JFET.

Applications of JFET

1. FET is used as a buffer in measuring instruments, receivers since it has high input impedance and low output impedance.
2. FET's are used in Radio Frequency amplifiers in FM (Frequency Mode) tuners and communication equipment for the low noise level.
3. Since the input capacitance is low, FET's are used in cascade amplifiers in measuring and test equipments.
4. Since the device is voltage controlled, it is used as voltage variable resistor in operational amplifiers and tone controls
5. FET's are used in mixer circuits in FM and TV receivers, and communication equipments because inter modulation distortion is low.
6. It is used in oscillator circuits because frequency drift is low.
7. As the coupling capacitor is small, FET's are used in low frequency amplifiers in hearing aids and inductive transducers.
8. FET's are used in digital circuits in computers, LSD and a memory circuit because of it is small size.

17.What are the types of MOSFET ? Explain the construction and working of Depletion MOSFET.

Ans: Depletion MOSFET works in two modes that are

1. Depletion mode
2. Enhancement mode

In depletion mode of operation the bias voltage on the gate reduce the number of charge carriers in the channel and therefore reduce the drain current.

In enhancement mode of operation the bias voltage on the gate increases the number of charge carriers in the channel and therefore increases the drain current.

The depletion MOSFET, operate in both depletion and enhancement modes whereas the enhancement MOSFET operate in enhancement mode only. In this section we study about depletion MOSFET.

4.23 Depletion MOSFET

The construction of n-channel depletion MOSFET is shown in Fig.4.40. It consists of a lightly doped p-type substrate in which two highly doped n-regions are diffused. The two heavily doped n-regions act as the source and drain. A lightly doped n-type channel is introduced between the two heavily doped source and drain. A thin layer of ($1\mu m$ thick) silicon dioxide is coated on the surface. Holes are cut in the oxide layer to make contact with n-regions. Due to Sio_2 layer the gate is completely insulated from the channel. This permits operation with gate-source or gate-channel voltages above and below zero. In addition, the insulating layer of Sio_2 accounts for very high input impedance of MOSFET. In some MOSFETs the p-type substrate is internally connected to source, whereas in many discrete devices an additional terminal is provided for substrate labeled SS (see Fig.4.40).

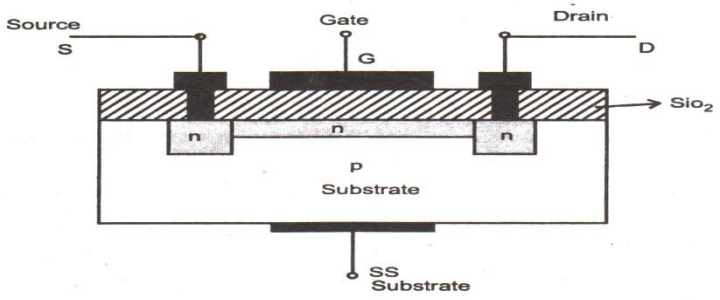


Fig. 4.40 n-channel depletion MOSFET

4.23.1 Basic Operation

In Fig.4.41 a voltage V_{DS} is applied between the drain and source terminal and the gate-to-source voltage is set to zero. As a result, current is established from drain to source (conventional direction) similar to that of JFET. Like in JFET, the saturated drain current I_{DSS} flows during pinch-off and it is labelled as I_{DSS}.

If a negative voltage is applied to gate with respect to source then holes are induced in the channel. These holes recombine with electrons and reduce the number of free electrons in the n-channel available for conduction. The more negative the bias, less the number of free electrons in the channel. Since the negative voltage on the gate deplete the channel the device is referred to as a depletion MOSFET. The depletion mode of operation similar to JFET operation. When sufficient negative voltage is applied to gate the channel may be completely cutoff and the corresponding V_{GS} is called ($V_{GS(OFF)}$).

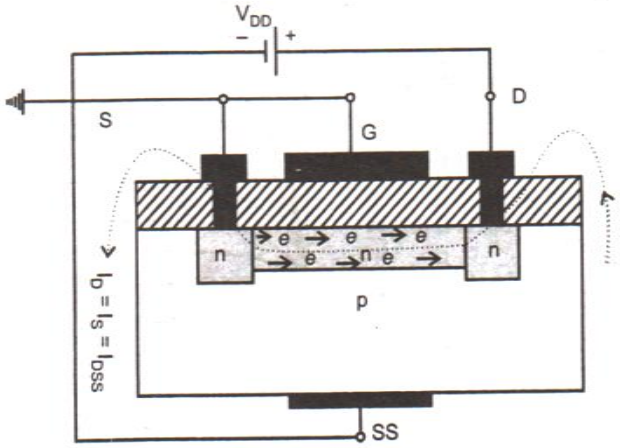


Fig. 4.41 n-channel depletion MOSFET with $V_{GS} = 0$ and applied voltage V_{DD}

If a positive voltage is applied to gate with respect to source then the electrons are induced in the channel. The induced electrons constitute additional current from source to drain. If we increase V_{GS} more in positive direction more number of electrons are induced, hence the drain current increases. That is the application of a positive gate-to-source voltage has enhanced the number of charge carriers compared to that of when $V_{GS} = 0V$. For this reason the mode in which the MOSFET operates for positive values of gate-to-source voltage is known as enhancement mode.

4.23.2 Characteristics of depletion MOSFET

Drain characteristics

It is a plot of drain current versus drain-source voltage for various value of gate-source voltage. The drain characteristics of depletion MOSFET is shown in Fig.4.42(b). Note that for negative of V_{GS} the characteristics of depletion MOSFET is similar to those N - channel JFET. If the gate is made positive additional carriers are introduced in the channel and the channel conductivity increases. Therefore, the depletion MOSFET consists of two regions of operation.

The transfer characteristics of depletion MOSFET is shown in Fig.4.42(a). The general shape of the transfer characteristics is similar to those for the JFET. However the depletion MOSFET can be operated with $V_{GS} > 0$. As a result I_{DSS} is not maximum drain current as it is for JFET. The equation for the transfer characteristics curve of depletion MOSFET is same as that of JFET.

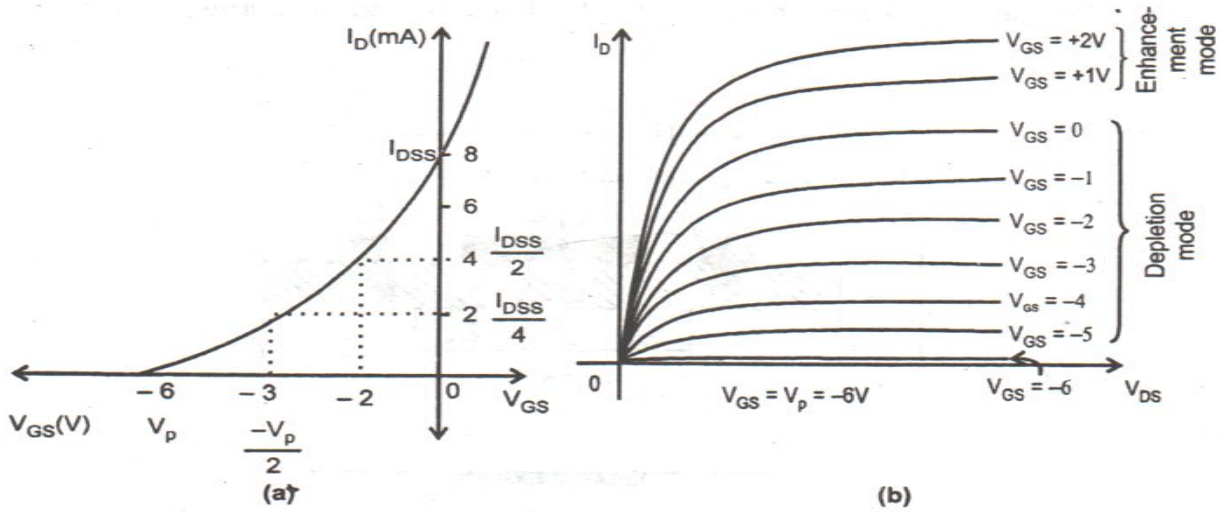


Fig. 4.42 (a) Transfer characteristics of N-channel depletion MOSFET (b) Drain characteristics of N-channel depletion MOSFET

18. Explain the construction and working of Enhancement MOSFET.

4.24 Enhancement MOSFET

The construction of n-channel enhancement MOSFET is shown in Fig.4.44. Like depletion MOSFET it also consists of a p-type substrate and two heavily doped n-regions that act as source and drain. The Sio_2 layer is present to isolate the gate from the region between the drain and source. The source and drain terminals are connected through metallic contacts to n-doped regions. But the enhancement MOSFET does not contain diffused channel between the source and drain (compare Fig.4.40 and Fig.4.44).

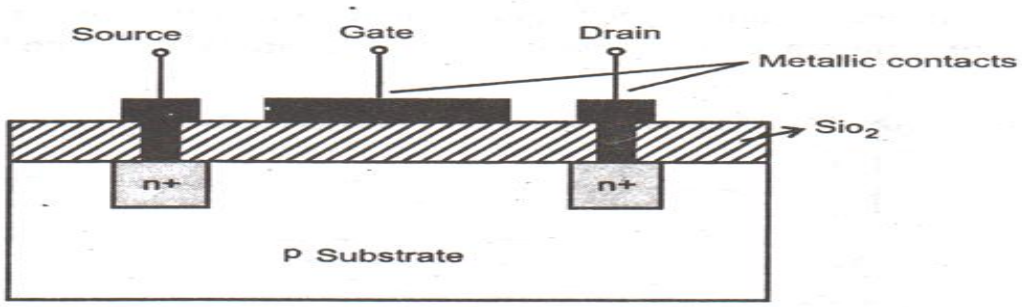


Fig. 4.44 Enhancement MOSFET

When the drain is made positive with respect to source and no potential is applied to gate, due to absence of the channel, a small drain current (i.e., a reverse leakage current) flows. If we apply a positive voltage to the gate with respect to source and substrate negative charge carriers are induced in the substrate. The negative charge

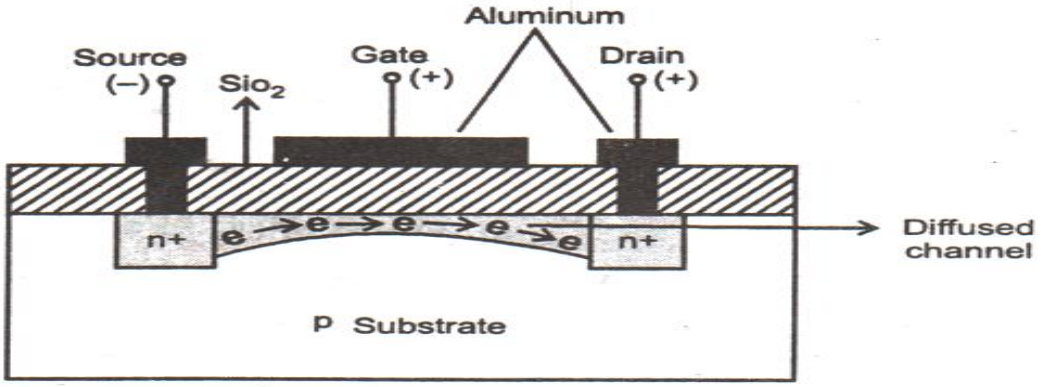


Fig. 4.45 Working of N-channel enhancement MOSFET

carriers which are minority carriers in the p-type substrate form a "inversion layer". As the gate potential is increased more and more negative charge carriers are induced. These negative carriers that are accumulated between source and drain constitute an n-type channel. Thus a drain current flows from source to drain through the induced channel. The magnitude of the drain current depends on the gate potential. Since the conduction of the channel is enhanced by the positive bias voltage on the gate the device is known as enhancement MOSFET.

4.24.1 Drain Characteristics

The drain characteristics of enhancement MOSFET is shown in Fig.4.46. The current I_{DSS} for $V_{GS} = 0$ is very small of the order of nano amperes shown in Fig.4.46. Note that the drain current increases with positive increase in gate source bias voltage.

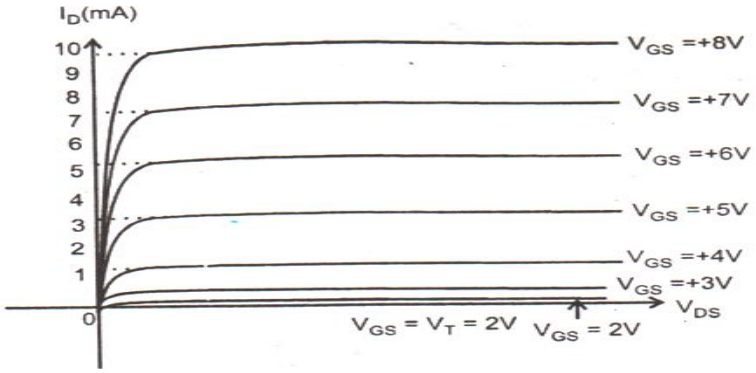


Fig. 4.46 Drain characteristics of n-channel enhancement MOSFET

4.24.2 Transfer characteristics

The n-channel enhancement MOSFET requires a positive gate to source voltage for its operation. Fig.4.47 shows the general transfer characteristics of an n-channel MOSFET . Since the drain current is zero for $V_{GS} = 0$, the I_{DSS} is zero for this device. As V_{GS} is made positive the current I_D increases slowly at first and then more rapidly with an increase in V_{GS}. The gate source voltage at which there is significant increase in drain current is called the threshold voltage and is referred to as V_T or $V_{GS(th)}$. The equation for the transfer characteristics of enhancement MOSFET differs the curve starts at $V_{GS(th)}$ rather than V_{GS}. Here the equation for transfer characteristics is

$$I_D = k(V_{GS} - V_{GS(\text{th})})^2$$

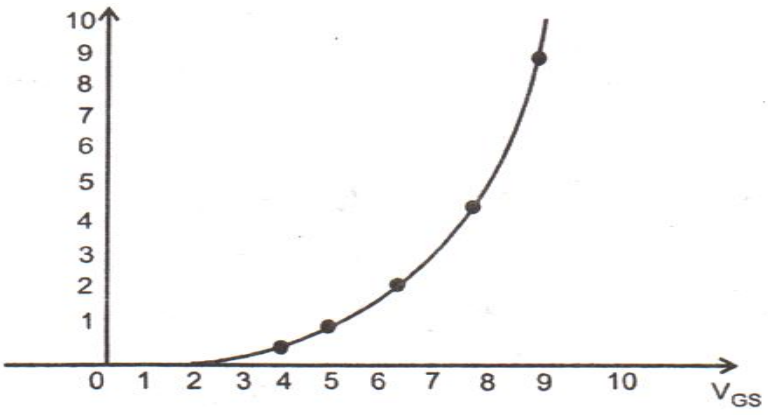


Fig. 4.47 Transfer characteristics of n-channel enhancement MOSFET

19. Compare JFET and MOSFET

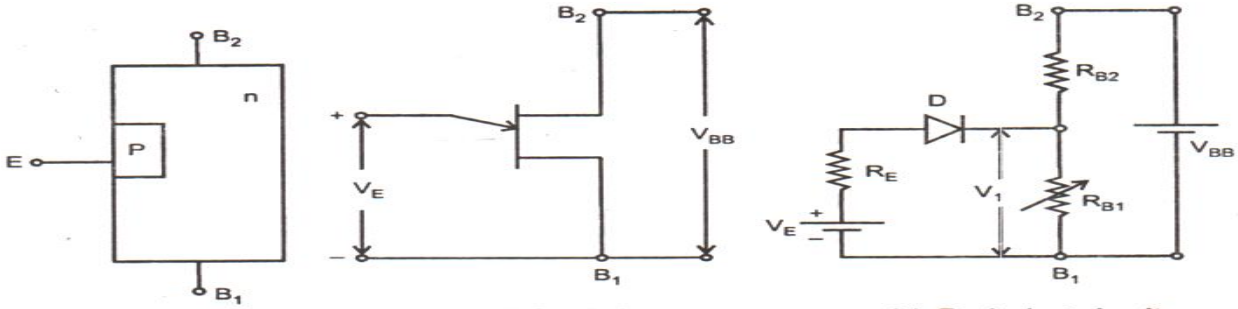
4.25 Comparison between MOSFET and JFET

	JFET	MOSFET
1.	The input resistance is the order of $10^9\Omega$ since there is no insulating layer between gate and the conducting channel.	The input resistance is very high in the order of $10^{13}\Omega$ due to presence of insulating layer between gate and conducting channel.
2.	The gate leakage current is the order of 0.1 to 10mA.	The gate leakage current is the order of 0.1 to 10PA.
3.	The drain resistance is the order of 0.1 to $1M\Omega$.	The drain resistance is the order of 1 to $50K\Omega$.
4.	Electric field across the reverse biased *pn* junction controls the conductivity of the channel.	Electric field across the insulating layer control the conductivity of the channel.
5.	Operates only in depletion mode.	The depletion mode MOSFET operates both in enhancement and depletion modes.
6.	V_{GS} for an n-channel JFET cannot be allowed to go positive since that would forward bias the gate source p-n junction and cause a large gate current to flow.	Gate source voltage of a depletion mode MOSFET can be negative or positive.

20. Explain the construction and working principle of UJT with its characteristics.

4.30 Unijunction Transistor (UJT)

The unijunction transistor (UJT) is a three terminal device. It consists of a slab of lightly doped n-type silicon material with two-end terminals base 1 (B_1) and base 2 (B_2). A heavily doped p-type material is injected to one side of the bar, which results in a p-n junction. The terminal connected to the p - n junction is termed as emitter (E). The symbol and equivalent circuit diagram of UJT is shown in Fig.(4.57)



(a) UJT construction (b) Symbol (c) Equivalent circuit

The n-type silicon bar has a resistance and can be represented as two resistors R_{B1} and R_{B2} in series. The resistance R_{B2} is fixed and the resistance R_{B1} is variable since its value varies with the operation of the device. The pn junction is represented by a diode. The arrow with in the symbol points the direction of conventional current (holes) flow when the device is forward biased. Hence it points from the p-type emitter to the n-type bar.

When emitter diode is non-conducting (when $I_E = 0$), the resistance between bases B_1 and B_2 is sum of R_{B1} and R_{B2}. That is $R_{BB} = R_{B1} + R_{B2}$ which is typically 5 to $10k\Omega$. When a supply voltage V_{BB} is applied between two bases the voltage across R_{B1} is given by

$$V_1 = V_{BB} \cdot \frac{R_{B1}}{R_{B1} + R_{B2}} = \frac{R_{B1}}{R_{BB}} V$$

$$V_1 = \eta V$$

where $$\eta = \frac{R_{B1}}{R_{BB}}$$

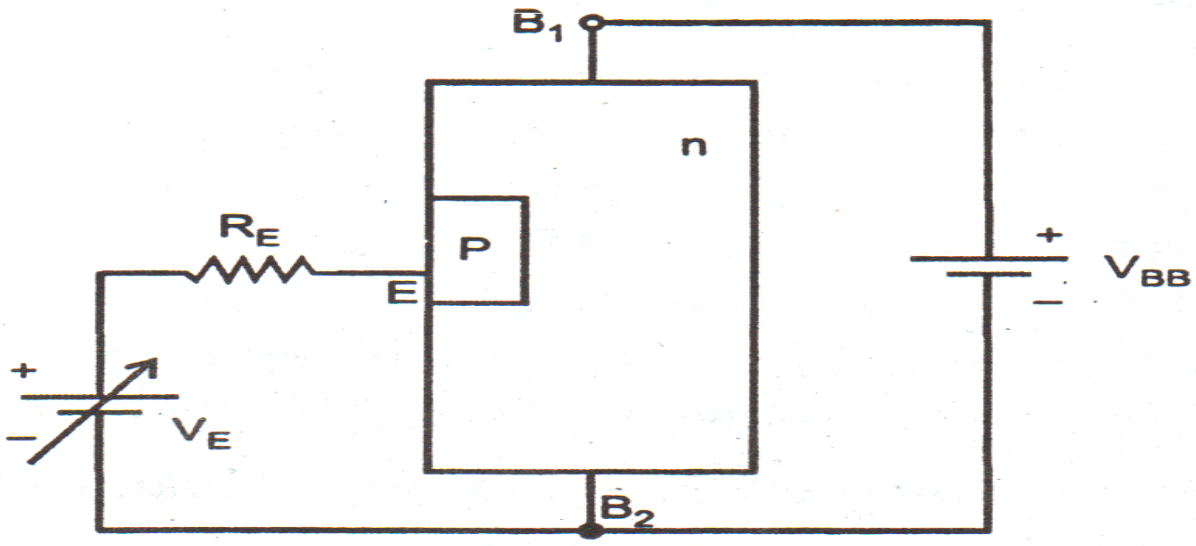
The quantity η is called the intrinsic stand off ratio. The typical range of η is from 0.5 to 0.8.

4.30.1 Working of UJT

When the applied voltage at the emitter is zero the reverse saturation current I_{EO} flows. The voltage $V_1 = \eta V_{BB}$ appears across the emitter diode. When a voltage V_E greater than V_1 by the forward voltage drop of the diode ($V_E > V_1 + 0.7$) is applied then the diode conducts. This voltage at which the diode conducts is known as peak voltage and is given by

$$V_P = \eta V_{BB} + V_D$$

The current flowing is termed as peak current I_P. When the pn junction is forward biased, charge carriers are injected into the R_{B1} region rapidly decreasing the resistance R_{B_1}. As a result the voltage drop across R_{B1} decreases causing the pn junction to be more heavily forward biased which in turn results in a greater forward current. Consequently more charge carriers are injected in R_{B1} region, increasing I_E. This increases the value of I_E up to a limit determined by the source resistance.



4.30.2 UJT Characteristics

The characteristics of UJT are shown in Fig.4.59. It is a plot between V_E and I_E keeping V_{BB} at a constant value. When $V_E = 0$, the emitter junction is reversed biased the emitter current I_{EO} flows. This reverse saturation current flows even we increase V_E up to V_P. This region in the characteristics is known as cut -off region. When $V_E = V_P$, the diodes starts conducting and the V_E will drop with increase in I_E establishing a negative resistance region as shown in Fig.4.59. In this region the resistance of R_{B1} falls rapidly and V_E falls to the valley voltage V_V. At this point I_E equals the valley current I_V. A further increase in I_E causes the device to enter the saturation region.

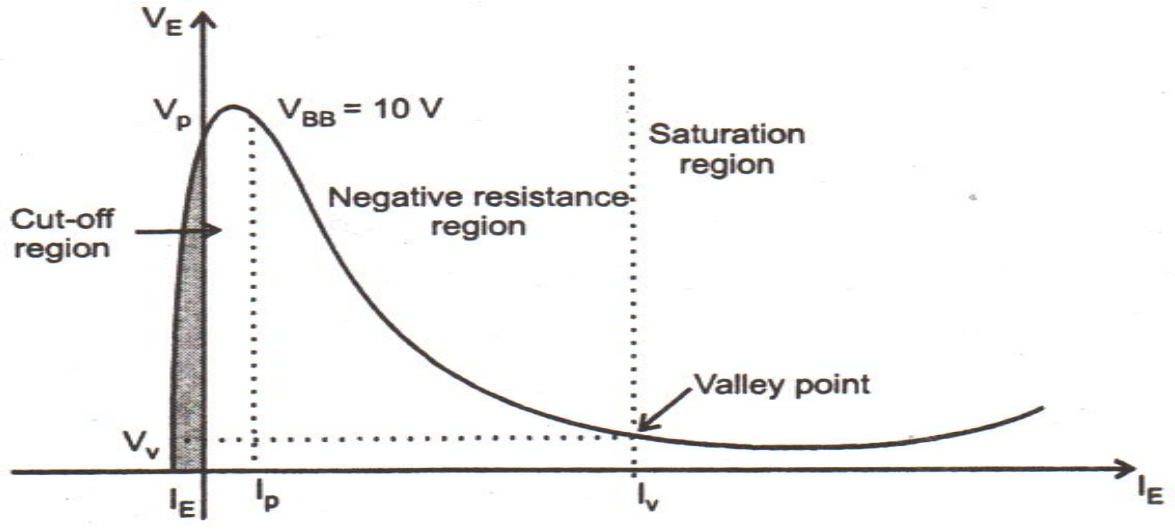


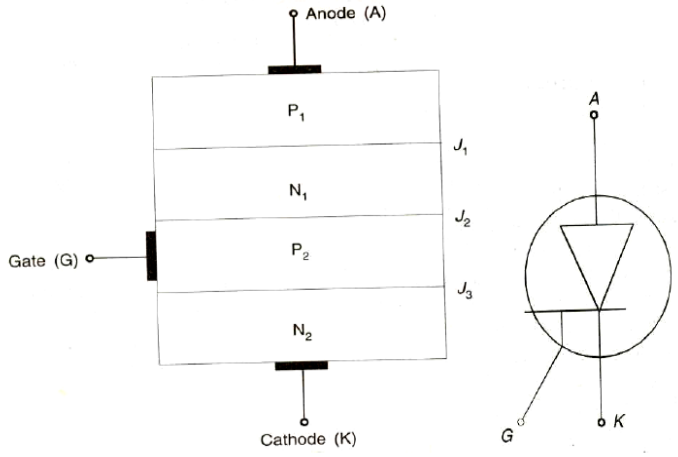
Fig. 4.59

21. Explain the working principle of SCR with its characteristics.

Ans:

SCR(Silicon Controlled Rectifier)

- It is an unidirectional device like diode, it allows to flow current in only one direction. But unlike diode, it has a built in features to switch ON and OFF.
- It is a 4 layer pnpn device where p & n layers are alternatively arranged. The outer layers are heavily doped.
- It has 3 terminals anode, cathode, gate and 3 p-n junctions called J_1, J_2 and J_3.
- The switching of SCR is controlled by the additional input called gate.



(a) Basic Structure (b) Circuit symbol

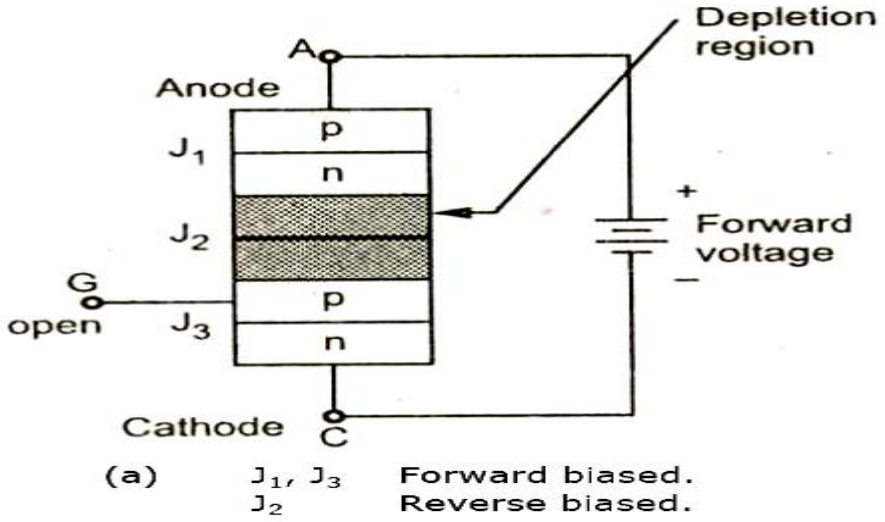
Fig, Basic structure and circuit symbol of SCR.

Operation of SCR:

The operation of SCR is divided into two categories,

i) When gate is open:

Consider that the anode is positive with respect to cathode and gate is open. The junctions J_1 and J_3 are forward biased and junctions J_2 is reverse biased. There is depletion region around J_2 and only leakage current flows which is negligibly small. Practically the SCR is said to be 'OFF'. This is called forward blocking state of SCR and voltage applied to anode and cathode with anode positive is called *forward voltage.* This is shown in figure (a) below.



2. When gate is closed:

Consider that the voltage is applied between gate and cathode when the SCR is in forward blocking state. The gate is made positive with respect to the cathode. The electrons from n-type cathode, which are majority in number, cross the junction J_3 to reach to positive of battery.

While holes from p-type move towards the negative of battery. This constitutes the gate current. This current increases the anode current as some of the electrons cross junction J_2. As anode current increases, more electrons cross the junction J_2 and the anode current further increases. Due to regenerative action, within short time, the junction J_2 breaks and SCR conducts heavily.

The connections are shown in the figure. The resistance R is required to limit the current.

Once the SCR conducts, the gate loses its control.

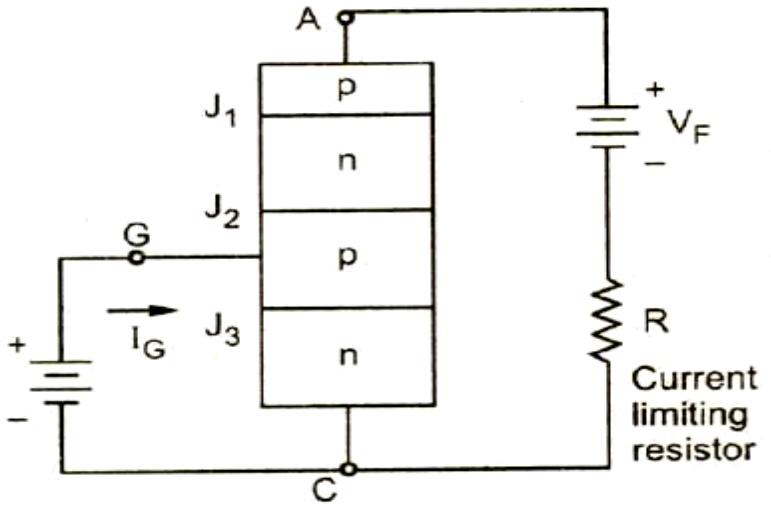


Fig. Operation of SCR when gate is closed.

Characteristics of SCR:

The characteristics are divided into two sections:

i) Forward characteristics

ii) Reverse characteristics

i) Forward characteristics:

It shows a forward blocking region, when I_G=0. It also shows that when forward voltage increases up to V_{BO}, the SCR turns ON and high current results. It also shows that, if gate bias is used then as gate current increases, less voltage is required to turn ON the SCR.

If the forward current falls below the level of the holding current I_H, then depletion region begins to develop around J_2 and device goes into the forward blocking region.

When SCR is turned on from OFF state, the resulting forward current is called *latching current* I_L. The latching current is slightly higher than the holding current.

ii) Reverse characteristics:

If the anode to cathode voltage is reversed, then the device enters into the reverse blocking region. The current is negligibly small and practically neglected.

If the reverse voltage is increases, similar to the diode, at a particular value avalanche breakdown occurs and a large current flows through the device. This is called reverse breakdown and the voltage at which this happens is called reverse breakdown voltage

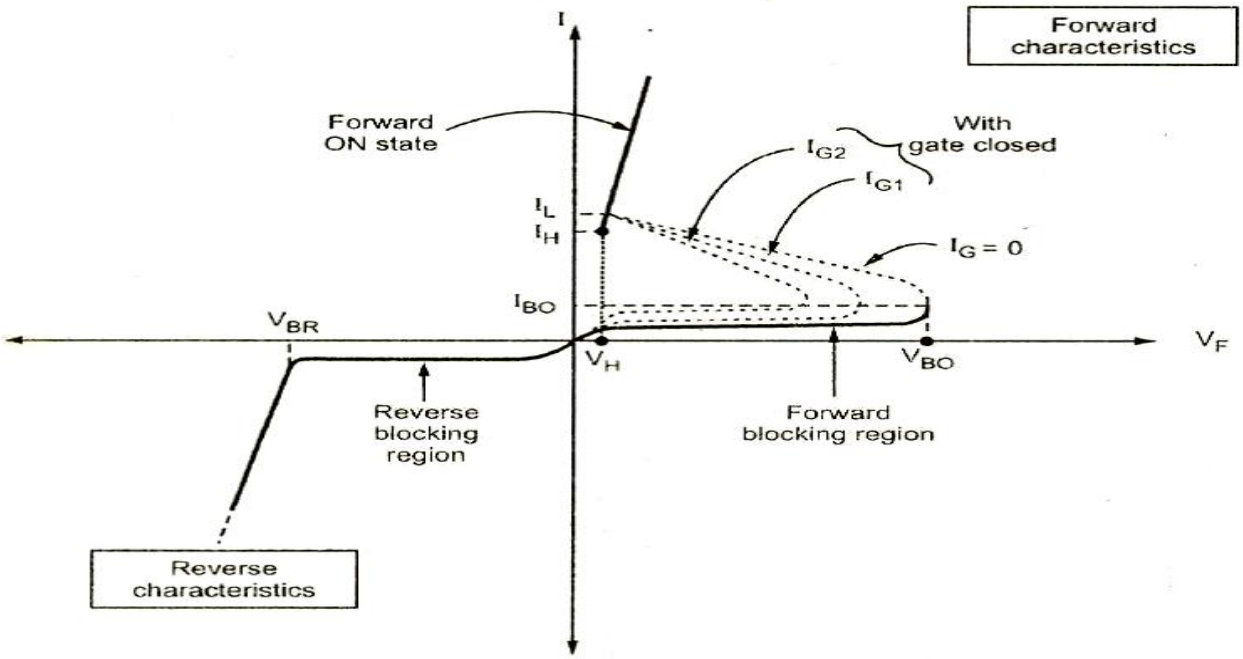


Fig. Characteristics of SCR.

Problem:1

In a common-base connection, the emitter current I_E is 6.28 mA and the collector current I_C is 6.20 mA. Determine the common-base d.c. current gain.

Solution:

Given: $I_E = 6.28$ mA and $I_C = 6.20$ mA

We know that common-base d.c. current gain,

$$\alpha = \frac{I_C}{I_E} = \frac{6.20 \times 10^{-3}}{6.28 \times 10^{-3}} = 0.987$$

Problem:2

The transistor has $I_E = 10$ mA and $\alpha = 0.98$. Determine the values of I_C and I_B.

Solution:

Given: $I_E = 10$ mA and $\alpha = 0.98$

The common-base d.c. current gain, $\alpha = \frac{I_C}{I_E}$

i.e. $0.98 = \frac{I_C}{10}$

Therefore $I_C = 0.98 \times 10 = 9.8$ mA

The emitter current $I_E = I_B + I_C$

i.e. $10 = I_B + 9.8$

Therefore, $I_B = 0.2$ mA

Problem3

A transistor has $\beta = 100$. If the collector current is 40 mA, find the value of emitter current.

Solution:

Given: $\beta = 100$ and $I_C = 40$ mA

$$\beta = 100 = \frac{I_C}{I_B} = \frac{40}{I_B}$$

Therefore, $I_B = 40/100 = 0.4$ mA and

$$I_E = I_B + I_C = (0.4 + 40) \times 10^{-3} = 40.4 \text{ mA}$$

Problem:4

A transistor has $I_B = 100$ μA and $I_C = 2$ mA. Find (a) β of the transistor, (b) α of the transistor, (c) emitter current I_E, (d) if I_B changes by + 25 μA and I_C changes by + 0.6 mA, find the new value of β.

Solution:

Given: $I_B = 100\ \mu\text{A} = 100 \times 10^{-6}$ A and $I_C = 2\ \text{mA} = 2 \times 10^{-3}$ A.

(a) **To find β of the transistor**

$$\beta = \frac{I_C}{I_B} = \frac{2 \times 10^{-3}}{100 \times 10^{-6}} = 20$$

(b) **To find α of the transistor**

$$\alpha = \frac{\beta}{\beta + 1} = \frac{20}{1 + 20} = 0.952$$

(c) **To find emitter current, I_E**

$$I_E = I_B + I_C = 100 \times 10^{-6} + 2 \times 10^{-3} \text{ A}$$
$$= (0.01 + 2) \times 10^{-3} = 2.01 \times 10^{-3} \text{ A} = 2.01 \text{ mA}$$

(d) **To find the new value of β when** $\Delta I_B = 25$ μA and $\Delta I_C = 0.6$ mA

Therefore, $I_B = (100 + 25)\ \mu\text{A} = 125\ \mu\text{A}$

$I_C = (2 + 0.6)\ \text{mA} = 2.6\ \text{mA}$

New value of β of the transistor,

$$\beta = \frac{I_C}{I_B} = \frac{2.6 \times 10^{-3}}{125 \times 10^{-6}} = 20.8$$

Problem:5

For a transistor circuit having $\alpha = 0.98$, $I_{CBO} = I_{CO} = 5$ μA and $I_B = 100$ μA, find I_C and I_E.

Solution:

Given: $\alpha = 0.98$, $I_{CBO} = I_{CO} = 5$ μA and $I_B = 100$ μA

The collector current is

$$I_C = \frac{\alpha \cdot I_B}{1 - \alpha} + \frac{I_{CO}}{1 - \alpha} = \frac{0.98 \times 100 \times 10^{-6}}{1 - 0.98} + \frac{5 \times 10^{-6}}{1 - 0.98} = 5.15 \text{ mA}$$

The emitter current is

$$I_E = I_B + I_C = 100 \times 10^{-6} + 5.15 \times 10^{-3} = 5.25 \text{ mA}$$

Problem:6

Determine I_C, I_E and α for a transistor circuit having $I_B = 15\ \mu A$ and $\beta = 150$.

Solution:

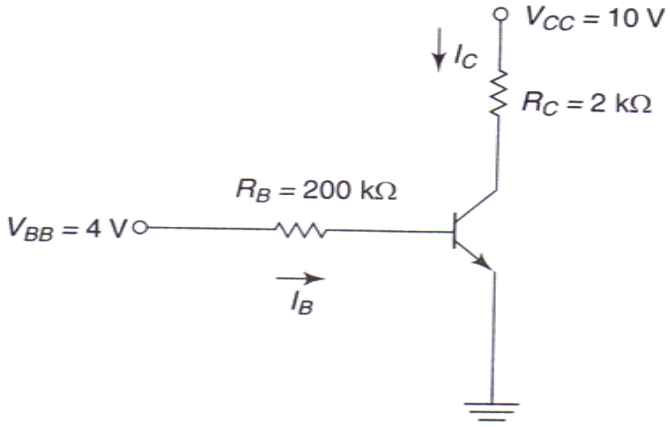
The collector current, $I_C = \beta I_B = 150 \times 15 \times 10^{-6} = 2.25\ mA$

The emitter current, $I_E = I_C + I_B = 2.25 \times 10^{-3} + 15 \times 10^{-6} = 2.265\ mA$

Common-base current gain, $\alpha = \dfrac{\beta}{1+\beta} = \dfrac{150}{151} = 0.9934$

Problem:7

Determine the base, collector and emitter currents and V_{CE} for a CE circuit shown in Fig. For $V_{CC} = 10$ V, $V_{BB} = 4$ V, $R_B = 200\ k\Omega$, $R_C = 2k\Omega$, V_{BE} (on) = 0.7 V, $\beta = 200$.



Solution:

Referring to Fig. 6.18, the base current is

$$I_B = \frac{V_{BB} - V_{BE}(on)}{R_B} = \frac{4 - 0.7}{200 \times 10^3} = 16.5\ \mu A$$

The collector current is

$$I_C = \beta I_B = 200 \times 16.5 \times 10^{-6} = 3.3\ mA$$

The emitter current is

$$I_E = I_C + I_B = 3.3 \times 10^{-3} + 16.5 \times 10^{-6} = 3.3165\ mA$$

Therefore, $V_{CE} = V_{CC} - I_C R_C = 10 - 3.3 \times 10^{-3} \times 2 \times 10^3 = 3.4$ V

Problem:8

Calculate the values of I_C and I_E for a transistor with $\alpha_{d.c.} = 0.99$ and $I_{CBO} = 5\ \mu A$. I_B is measured as 20 μA.

Solution:

Given, $\alpha_{d.c.} = 0.99$, $I_{CBO} = 5\ \mu A$ and $I_B = 20\ \mu A$

$$I_C = \frac{\alpha_{d.c.} I_B}{1-\alpha_{d.c.}} + \frac{I_{CBO}}{1-\alpha_{d.c.}} = \frac{0.99 \times 20 \times 10^{-6}}{1-0.99} + \frac{5 \times 10^{-6}}{1-0.99} = 2.48\ mA$$

Therefore, $I_E = I_B + I_C = 20 \times 10^{-6} + 2.48 \times 10^{-3} = 2.5\ mA$

Problem:9

When a reverse gate voltage of 12 V is applied to JFET, the gate current is 1 nA. Determine the resistance between gate and source.

Solution: $V_{GS} = 12\ V$, $I_G = 10^{-9}\ A$.

Therefore, gate-to-source resistance $= \frac{V_{GS}}{I_G} = \frac{12}{10^{-9}} = 12{,}000\ M\Omega$

Problem10

When the reverse gate voltage of JFET changes from 4.0 to 3.9 V, the drain current changes from 1.3 to 1.6 mA. Find the value of transconductance.

Solution: $\Delta V_{GS} = 4.0 - 3.9 = 0.1\ V$

$\Delta I_D = 1.6 - 1.3 = 0.3\ mA$

Therefore, transconductance, $g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3 \times 10^{-3}}{0.1} = 3\ m\ mho$.

Problem11

A FET has a driven current of 4 mA. If $D_{SS} = 8$ mA and $V_{GS(off)} = -6$ V. Find the values of V_{GS} and V_P.

Solution:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$4 = 8\left[1 + \frac{V_{GS}}{6}\right]^2$$

$$1 + \frac{V_{GS}}{6} = \sqrt{\frac{4}{8}} = \frac{1}{\sqrt{2}} = 0.707$$

Therefore, $V_{GS} = -1.76\ V$

$V_P = |V_{GS(off)}| = 6V$

Problem12

An N-channel JFET has I_{DSS} = 8 mA and V_p = –5 V. Determine the minimum value of V_{DS} for pinch-off region and the drain current I_{DS}, for V_{GS} = – 2 V in the pinch-off region.

Solution: The minimum value of V_{DS} for pinch-off to occur for V_{GS} = – 2 V is

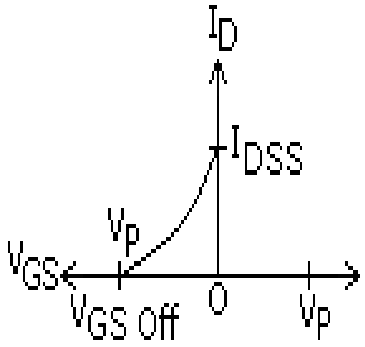
$$V_{DSmin} = V_{GS} - V_P = -2 - (-5) = 3V$$

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 8 \times 10^{-3}\,[1 - (-2)/(-5)]^2 = 2.88 \text{ mA}$$

Problem13

A FET has a drain current of 4mA. If I_{DSS} = 8mA and V_{GS} off = -6V. Find values of V_{GS} and V_P.



Given IDS = 4 mA
IDSS = 8mA
V_{GSoff} = - 6V.
Ans: (i) VP = V_{GSoff} = -6V = 6V.

(ii) $I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$

$4\times10^{-3}=8\times10^{-3}\left[1 - \frac{V_{GS}}{6}\right]^2$

$\frac{1}{2} = \left[1 - \frac{V_{GS}}{6}\right]^2$

V_{GS}= 6 0.293 1.758 Volts

Problem14.

The readings obtained from a JFET are as follows: -
Drain to source voltage (volts) = 5 12 12
Gate to source voltage (volts) = 0 0 -0.25
Drain current Id (mA) = 8 8.2 7.5
Determine (i) AC drain resistance (ii) TransConductance (iii) Amplification Factor

SOL:

(i) **Ac Drain Resistance** = $r_D = \frac{\Delta V_{DS}}{\Delta I_D}|_{V_{Gs}=Constant}$

$$= \frac{12-5\ (\text{Volts})}{8.2-8(\text{mA})} = \frac{7}{0.2\times10^{-3}} = 35\ \text{K}\Omega.$$

(ii) **Transconductance** = $\frac{\Delta I_D}{\Delta V_{GS}}|_{V_{DS}=Constant} = \frac{8.2-7.5}{0-(-0.25)} = \frac{0.7\text{mA}}{0.25} = 2.8\text{m}\mho$

(iii) **Amplification Factor,** $\mu = r_D \times g_m = 2.8 \times 10^{-3} \times 35 \times 10^3 = 98$

Biasing and Stabilization

1. What is the use of biasing? Draw the DC equivalent model.

Ans: TRANSISTOR BIASING

The basic function transistor is to do amplification. The process of raising the strength of a weak signal without any change in its shape is known as faithful amplification. For faithful amplification, the following three conditions must be satisfied:

i) The emitter-base junction should be forward biased,

ii) The collector-base junction should be reverse biased.

iii) Three should be proper zero signal collector current.

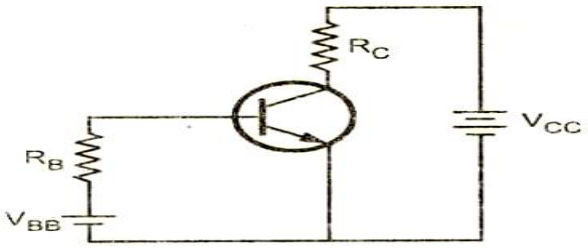
The proper flow of zero signal collector current (proper operating point of a transistor) and the maintenance of proper collector-emitter voltage during the passage of signal is known as 'transistor biasing'.

In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chose. These voltages and resistances establish a set of d.c. voltage V_{CEQ} and current I_{CQ} to operate the transistor in the active region. These voltages and currents are called quiescent values which determine the operating point (or) Q-Point for the transistor.

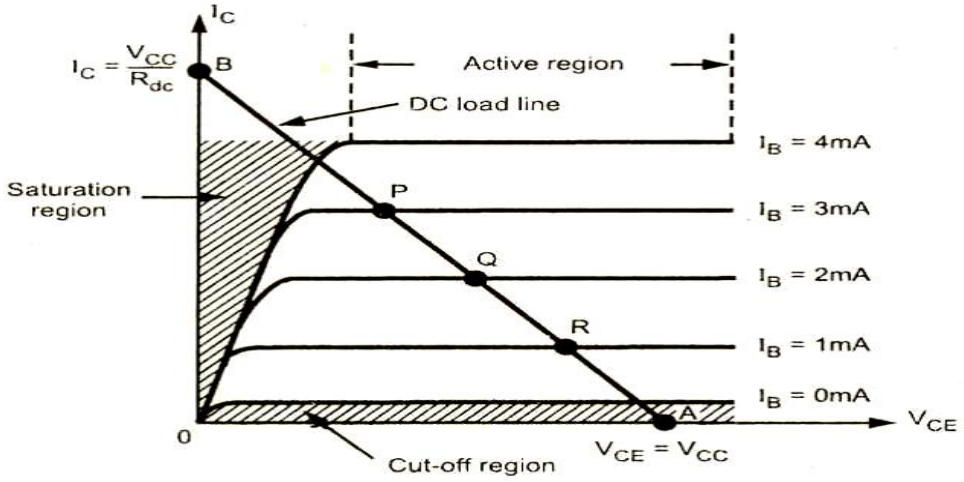
The process of giving proper supply voltages and resistances for obtaining the desired Q Point is called biasing.

DC Load Line:

Consider common emitter configuration circuit shown in figure below:



In transistor circuit analysis generally it is required to determine the value of I_C for any desired value of V_{CE}. From the load line method, we can determine the value of I_C for any desired value of V_{CE}. The output characteristics of CE configuration is shown in figure below:



By applying KVL to the collector circuit

$$-V_C + I_C R_C + V_{CE} = 0$$

$$\Rightarrow V_{CC} = I_C R_C + V_{CE}$$
$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

If the bias voltage V_{BB} is such that the transistor is not conducting then $I_C=0$ and $V_{CE}= V_{CC}$.
Therefore, when $I_C=0$, $V_{CE}= V_{CC}$ this point is plotted on the output characteristics as point A.

If $V_{CE}=0$ then

$$0 = V_{CC} - I_C R_C$$
$$\Rightarrow I_C = \frac{V_{CC}}{R_C}$$

Therefore, $V_{CE}=0$, $I_C = \frac{V_{CC}}{R_C}$ this point is plotted on the output characteristics as point B.

The line drawn through these points is straight line 'd.c load line'.

The d.c. load line is plot of I_C versus V_{CE} for a given value of R_C and a given level of V_{CC}. Hence from the load line we can determine the I_C for any desired value of V_{CE}.

Operating Point (or) Quiescent Point:

In designing a circuit, a point on the load line is selected as the dc bias point (or) quiescent point. The Q-Point specifies the collector current I_C and collector to emitter voltage V_{CE} that exists when no input signal is applied. The dc bias point (or) quiescent point is the point on the load line which represents the current in a transistor and the voltage across it when no signal is applied. The zero signal values of I_C ad V_{CE} are known as the operating point.

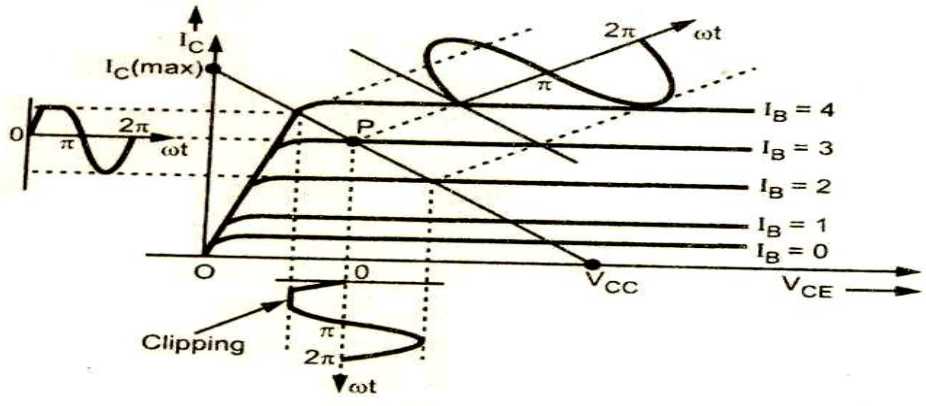
Biasing:

The process of giving proper supply voltages and resistances for obtaining the desired Q point is called 'biasing'.

2. **Explain the criteria for fixing operating point. (or) Explain the reasons for keeping the operating point of a transistor as fixed.**

Ans:

- The operating point can be selected at three different positions on dc load line: near saturation region, near cut-off region or at the center, i.e. in the active region.
- The selection of operating point will depend on its application. When transistor is used as an amplifier, the Q point should be selected at the center of the dc load line to prevent any possible distortion in the amplified output signal. This is well-understood by going through following cases.
- **Case 1:** Biasing circuit is designed to fix a Q-point at point P, as shown in fig.(a). point P is very near to the saturation region. The collector current is clipped at the positive half cycle. So, even though base current varies sinusoid ally, collector current is not a useful sinusoidal waveform. i.e. distortion is present at the output. Therefore, point P is not a suitable operating point.



Fig(a). Operating point near saturation region gives clipping at the positive peak.

- **Case 2:** In fig.(b) shows biasing circuit is designed to fix a Q point at point R is very near to the cut-off region. The collector current is clipped at the negative half cycle. So, point R is also not a suitable operating point.

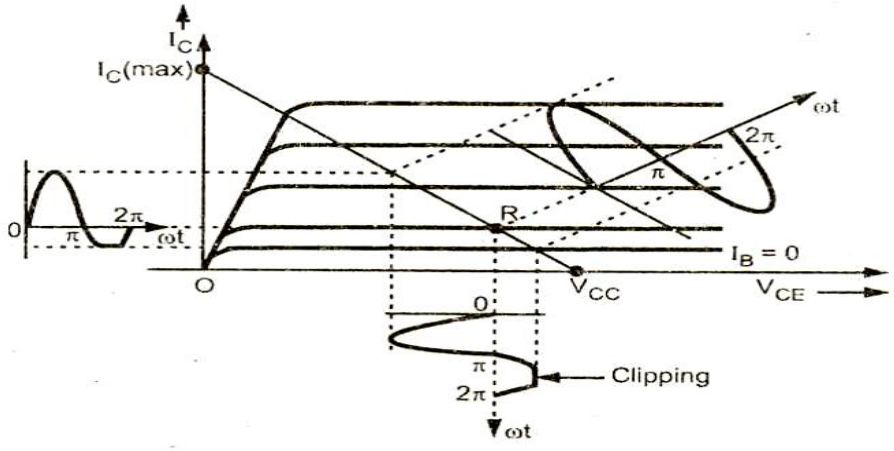
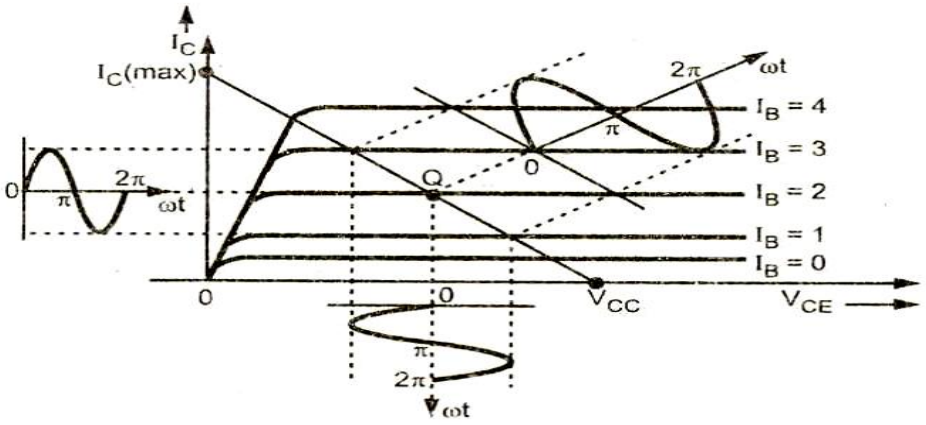


Fig.(b) Operating point near cut-off region given clipping at the negative peak.

- **Case 3:** Biasing circuit is designed to fix a Q-point at point Q as shown in fig.(c). The output signal is sinusoidal waveform without any distortion. Thus point Q is the best operating point.



Fig(c). Operating point at the centre of active region is most suitable.

3. Define stability factors S, S' and S''

Stability factors:

Since there are three variables which are temperature dependent, we can define three stability factors as below:

i) S: The stability factor 'S' is defined as the ration of change of collector current I_C with respect to the reverse saturation current I_{CO}, keeping β and V_{BE} constant.

$$\text{i.e.,} \quad S = \frac{\partial I_C}{\partial I_{CO}} \approx \left.\frac{\partial I_C}{\partial I_{CO}}\right| \quad V_{BE},\ \beta \text{ constant}$$

ii) **S':** The stability factor S' is defined as the rate of change of I_C with respect to V_{BE}, keeping I_{CO} and β constant i.e.,

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \left.\frac{\partial I_C}{\partial V_{BE}}\right| \quad I_{CO},\ \beta \text{ constant}$$

iii) **S'':** The stability factor S'' is defined as the rate of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant i.e.,

$$S' = \frac{\partial I_C}{\partial \beta} \approx \left.\frac{\partial I_C}{\partial \beta}\right| \quad I_{CO},\ V_{BE} \text{ constant}$$

Ideally, stability factor should be perfectly zero to keep operating point stable.

Practically, stability factor should have the value as minimum as possible.

Derivation of Stability Factor (S):

For a common emitter configuration collector current is given as,

$$I_C = \beta I_B + I_{CEO}$$

$$\Rightarrow I_C = \beta I_B + (1+\beta) I_{CO} \qquad \text{..... (1)}$$

Differentiating equation (1) w.r.t. I_C keeping β constant, we get

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$$

$$\Rightarrow 1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$$

$$\Rightarrow \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

$$\Rightarrow S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}} \qquad \text{..... (2)}$$

4. List out the different types of biasing methods. Explain about collector to base bias circuit.

Ans: Methods of Biasing:

Some of the methods used for providing bias for a transistor are as follows:

1) Fixed bias (or) base resistor method.

2) Collector to base bias (or) biasing with feedback resistor.

3) Voltage divider bias (or) Self bias.

Collector to Base bias (or) Biasing with feedback resistor:

A CE amplifier using collector to base bias circuit is shown in the figure. In this method, the biasing resistor is connected between the collector and the base of the transistor.

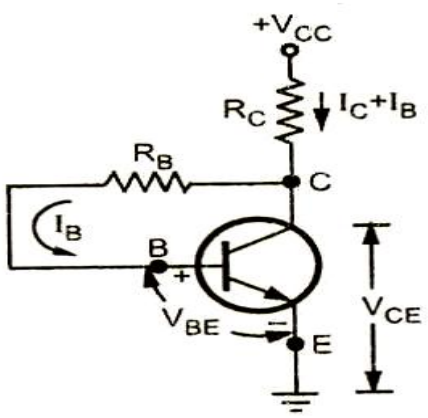


Fig. Collector–to–Base bias circuit.

Circuit Analysis:
Base Circuit:

Consider the base-emitter circuit, applying the KVL to the circuit we get,

$$V_{CC} - \left(I_B + I_C\right) R_C - I_B R_B - V_{BE} = 0$$

$$\Rightarrow V_{CC} = I_B \left(R_C + R_B\right) + I_C R_C + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \qquad \text{..... (1)}$$

But $I_C = \beta I_B$

$$\therefore I_C = \frac{\beta\left(V_{CC} - I_C R_C - V_{BE}\right)}{R_C + R_B} \qquad \text{..... (2)}$$

Collector circuit:

Consider the collector-emitter circuit, applying the KVL to the circuit we get

$$-V_{CC} + \left(I_B + I_C\right) R_C + V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - \left(I_C + I_B\right) R_C \qquad \text{..... (3)}$$

Stability factor S:

The stability factor S is given by,

$$S = \frac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}}$$

We have $I_B = \dfrac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$ = constant

Differentiating the above equation w.r.t. I_C we get

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_C + R_B}$$

$$\therefore S = \frac{1+\beta}{1+\beta\dfrac{R_C}{R_C+R_B}} \qquad \text{..... (4)}$$

The stability factor S is smaller than the value obtained by fixed bias circuit. Also 'S' can be made smaller by making R_B small (or) R_C large.

5. Draw a BJT fixed bias circuit and derive the expression for the stability factor 'S'.

1). Fixed bias (or) base resistor method:

A CE amplifier used fixed bias circuit is shown in figure below:

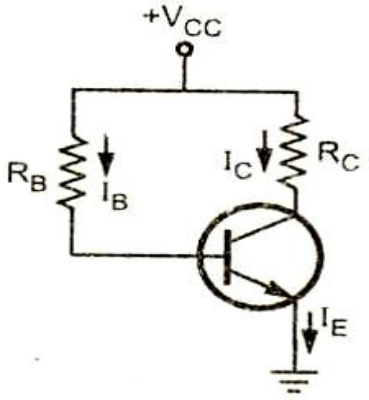


Fig. Fixed bias circuit.

In this method, a high resistance R_B is connected between positive terminal of supply V_{CC} and base of the transistor. Here the required zero signal base current flows through R_B and is provided by V_{CC}.

In figure, the base-emitter junction is forward biased because the base is positive w.r.t. emitter. By a proper selection of R_B, the required zero signal base current (and hence $I_C=\beta I_B$) can be made to flow.

Circuit Analysis:

Base Circuit:

Consider the base-emitter circuit loop of the above figure.

Writing KVL to the loop, we obtain

$$-V_{CC} + I_B R_B + V_{BE} = 0$$

$$\Rightarrow V_{CC} = I_B R_B + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

But $I_C = \beta I_B + I_{CEO}$

As I_{CEO} is very small, $I_C \approx \beta I_B$

$$\therefore I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

$\Rightarrow$ β, V_{CC}, V_{BE} are constant for a transistor $\therefore$ I_C depends on R_B.

Choose suitable value of R_B to get constant I_C in active region.

$$\therefore R_B = \frac{(V_{CC} - V_{BE})\beta}{I_C} \quad \text{(or)} \quad R_B = \frac{\beta V_{CC}}{I_C} \qquad (\because V_{BE} << V_{CC})$$

Collector Circuit:

Consider the collector-emitter circuit loop of the circuit.

Writing KVL to the collector circuit, we get

$$-V_{CC} + I_B R_B + V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

Stability factor S:

The stability factor S is given by, $$S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

We have $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ = constant $\therefore \frac{\partial I_B}{\partial I_C} = 0$

$$\therefore S = 1 + \beta$$

If β=100 then S=101. This shows that I_C changes 101 times as much as any changes in I_{CO}. Thus I_C is dependent upon I_{CO} and temperature.

The value of S is high and has very poor stability.

Advantages of fixed bias circuit:

1. This is a simple circuit which uses very few components.
2. The operating point can be fixed anywhere in the active region of the characteristics by simply changing the values of R_B. Thus, it provides maximum flexibility in the design.

Disadvantages of fixed bias circuit:

1. With the rise in temperature the operating point is not stable.
2. When the transistor is replaced by another with different value of β, the operating point with shift i.e., the stabilization of operating point is very poor in fixed bias circuit.

6. Draw the circuit diagram of a self bias BJT circuit and how to determine the values of R_1 and R_2.

Voltage Divider Bias (Or) Self-Bias (Or) Emitter Bias:

The voltage divider bias circuit is shown in figure.

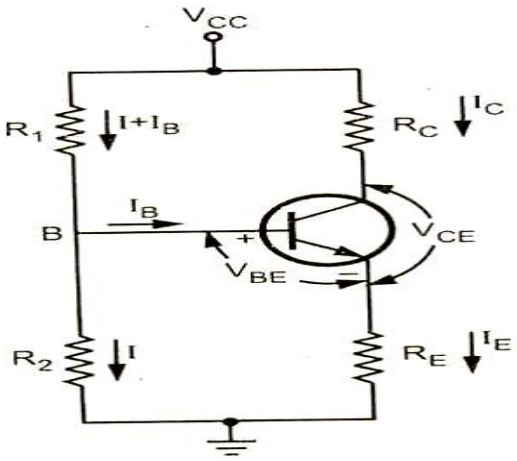


Fig: Voltage devider bias circuit

In this method, the biasing is provided by three resistors R_1, R_2 and R_E. The resistors R_1 and R_2 acts as a potential divider giving a fixed voltage to the base. If collector current increases due to change in temperature (or) change in β, the emitter current I_E also increases and the voltage drop across R_E increases, reducing the voltage difference between base and emitter (V_{BE}).

Due to reduction in V_{BE}, base current I_B and hence collector current I_C is also reduces. Therefore, we can say that negative feedback exists in the emitter bias circuit. This reduction in collector current I_C components for the original change in I_C.

Circuit analysis using Thevenin's Theorem:

The Thevenin equivalent circuit of voltage-divider bias is as shown below:

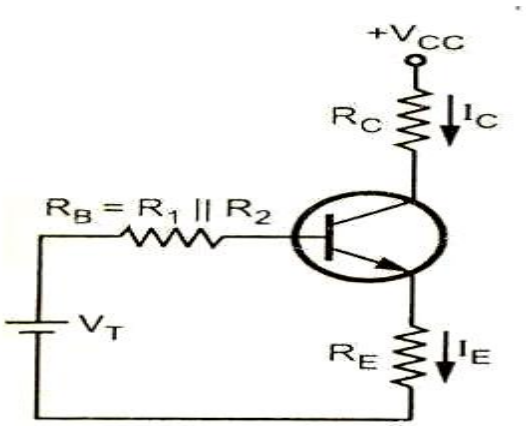


Fig. Thevenin's equivalent circuit.

From above figure we have,

$$V_2 = V_{Th} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} \qquad \text{..... (5)}$$

$$R_{Th} = R_1 \square R_2 = \frac{R_1 R_2}{R_1 + R_2} \qquad \text{..... (6)}$$

Applying KVL to the base-emitter circuit, we have

$$V_{Th} = I_B R_{Th} + V_{BE} + (I_B + I_C) R_E \qquad \text{..... (7)}$$

Applying KVL to the collector-emitter circuit, we have

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \qquad (\because I_C >> I_B) \quad \text{.....(8)}$$

From equation (8), we have

$$\therefore I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

Substituting this value of I_C in equation (7), we have

$$V_{Th} = I_B R_{Th} + V_{BE} + R_E \left[I_B + \frac{V_{CC} - V_{CE}}{R_C + R_E} \right]$$

$$V_{Th} = I_B R_{Th} + V_{BE} + R_E I_B + \frac{R_E V_{CC}}{R_C + R_E} - \frac{R_E V_{CE}}{R_C + R_E}$$

Stability factor (S):

For determining stability factor 'S' for voltage divider bias, consider the Thevenin's equivalent circuit. Hence, Thevenin's equivalent voltage V_{th} is given by

$$V_{Th} = \frac{R_2}{R_1 + R_2} V_{CC}$$

and the R1 and R2 are replaced by R_B which is the parallel combination of R_1 and R_2.

$$\therefore R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Applying KVL to the base circuit, we get

$$V_{Th} = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating w.r.t. I_C and considering V_{BE} to be independent of I_C we get,

$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} (R_E) + R_E$$

$$\therefore \frac{\partial I_B}{\partial I_C} (R_E + R_B) = -R_E \qquad \therefore \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B}$$

We have already seen the generalized expression for stability factor 'S' given by

$$S = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

Substituting value of $\frac{\partial I_B}{\partial I_C}$ in the above equation, we get

$$\therefore S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$$

$$\Rightarrow S = \frac{(1+\beta)(R_E+R_B)}{R_B+R_E+\beta R_E} = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E}$$

$$S = (1+\beta)\left(\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}}\right)$$

The ratio $\frac{R_B}{R_E}$ controls value of stability factor 'S'.

If $\frac{R_B}{R_E} << 1$ then above equation reduces to $S = (1+\beta)\left(\frac{1}{1+\beta}\right) = 1$

Practically $\frac{R_B}{R_E} \neq 0$ But to have better stability factor 'S', we have to keep ration $\frac{R_B}{R_E}$ as small as possible.

Stability factor 'S' for voltage divider bias (or) self bias is less as compared to other biasing circuits studied. So, this circuit is most commonly used.

7. What are the compensation techniques used for V_{BE} and I_{CO}? Explain with the help of suitable circuits.

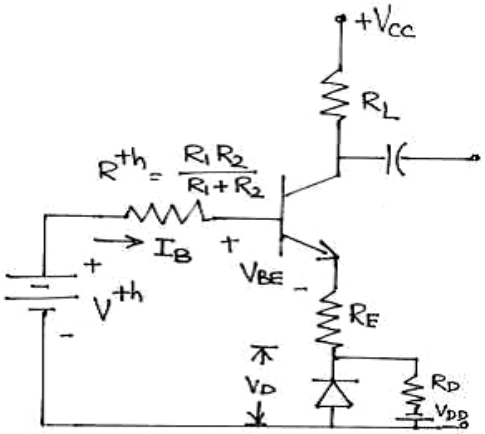
Ans: The stabilization techniques refer to the use of resistive biasing circuits which permit I_B to vary so as to keep I_C relatively constant. On the other hand, compensation techniques refer to the use of temperature sensitive devices such as diodes, transistors, thermistors, sensistors etc., to compensate for the variation in currents. Sometimes for excellent bias and thermal stabilization, both stabilization as well as compensation techniques are used.

The following are some compensation techniques:

1) Diode compensation for instability due to V_{BE} variation.
2) Diode compensation for instability due to I_{CO} variation.
3) Thermistor compensation.
4) Sensistor compensation.

1) Diode compensation for instability due to V_{BE} variation:

For germanium transistor, changes in I_{CO} with temperature contribute more serious problem than for silicon transistor. On the other hand, in a silicon transistor, the changes of V_{BE} with temperature possesses significantly to the changes in I_C. A diode may be used as compensation element for variation in V_{BE} (or) I_{CO}. The figure below shows the circuit of self bias stabilization technique with a diode compensation for V_{BE}. The Thevenin's equivalent circuit is shown in figure.



The diode D used here is of the same material and type as the transistor. Hence the voltage V_D across the diode has same temperature coefficient (-2.5mV/^oC) as V_{BE} of the transistor. The diode D is forward biased by the source V_{DD} and resistor R_D.

Applying KVL to the base circuit, we get

$$-V_{th} + I_B R_{th} + V_{BE} + I_E R_E - V_D = 0$$

$$\Rightarrow \quad V_{th} - V_{BE} + V_D = I_B R_{th} + R_E(I_E + I_C) \cdots\cdots\cdots (1)$$

But $$I_C = \beta I_B + (1+\beta) I_{CO} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (2)$$

From equation (1), we get

$$V_{th} - V_{BE} + V_D = R_E I_C + (R_{th} + R_E) I_B$$

Substituting value of I_B from equation (2), we get

$$V_{th} - V_{BE} + V_D = R_E I_C + (R_{th} + R_E)\left[\frac{I_C - (1+\beta) I_{CO}}{\beta}\right]$$

$$\Rightarrow \quad \beta(V_{th} - V_{BE} + V_D) = \beta R_E I_C + (R_{th} + R_E) I_C - (1+\beta) I_{CO}(R_{th} + R_E)$$

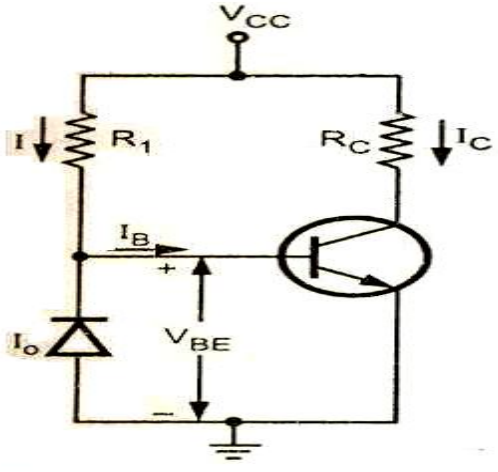
$$\Rightarrow \quad \beta(V_{th} - V_{BE} + V_D) = (1+\beta) I_{CO}(R_{th} + R_E) = I_C(R_{th} + (1+\beta) R_E)$$

$$\Rightarrow \quad I_C = \frac{\beta(V_{th} - V_{BE} + V_D) = (1+\beta) I_{CO}(R_{th} + R_E)}{R_{th} + (1+\beta) R_E} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (3)$$

Since variation in V_{BE} with temperature is the same as the variation in V_D with temperature, hence the quantity (V_{BE}-V_D) remains constant in equation (3). So the current I_C remains constant in spite of the variation in V_{BE}.

2) Diode compensation for instability due to I_{CO} variation:

Consider the transistor amplifier circuit with diode D used for compensation of variation in I_{CO}. The diode D and the transistor are of the same type and same material.



In this circuit diode is kept in reverse biased condition. The reverse saturation current I_O of the diode will increase with temperature at the same as the transistor collector saturation current I_{CO}.

From figure $I = \frac{V_{CC} - V_{BE}}{R} \approx \frac{V_{cc}}{R} = constant$

The diode D is reverse biased by V_{BE}. So the current through D is the reverse saturation current I_O. Now base current $I_B = I - I_O$

But $I_C = \beta I_B + (1+\beta) I_{CO}$

$\Rightarrow I_C = \beta(I - I_O) + (1+\beta) I_{CO}$

If $\beta \gg 1, I_C \approx \beta I - \beta I_O + \beta I_{CO}$

In the above expression, I is almost constant and if I_O of diode D and I_{CO} of transistor track each other over the operating temperature range, then I_C remains constant.

8. Explain in detail about themal runaway and thermal resistance.

Ans: Thermal Runaway:

The collector current for the CE circuit is given by $I_C = \beta I_B + (1+\beta) I_{CO}$ The three variables in the equation, β, I_B and I_{CO} increase with rise in temperature. In particular, the reverse saturation current (or) leakage current I_{CO} changes greatly with temperature. Specifically, it doubles for every ^{10oC} rise in temperature. The collector current I_C causes the collector-base junction temperature to rise which, in turn, increase I_{CO}, as a result I_C increase still further, which will further rise the temperature at the collector-base junction. This process is cumulative and it is referred to as self heating. The excess heat produced at the collector-base junction may even burn and destroy the transistor. This situation is called "Thermal Runaway" of the transistor.

Thermal Resistance:

Transistor is a temperature dependent device. In order to keep the temperature within the limits, the heat generated must be dissipated to the surroundings. Most of the heat within the transistor is produced at the collector junction. If the temperature exceeds the permissible limit,the junction is destroyed. For Silicon transistor, the temperature is in the range 150^o C to 225^o C. For Germanium, it is between 60^o C to 100^o C.

Let T_A ^{o}C be the ambient temperature i.e., the temperature of surroundings air around transistor and T_J ^{o}C, the temperature of collector-base junction of the transistor.

Let P_D be the power in watt dissipated at the collector junction. The steady state temperature rise at the collector junction is proportional to the power dissipated at the junction. It is given by

$$\partial T = T_J - T_A = \theta P_D$$

Where θ = constant of proportionality. Which is referred to as thermal resistance.

$$\theta = \frac{T_J - T_A}{P_D}$$

The unit of θ, the thermal resistance, is ^{o}C/watt.

The typical values of θ for various transistors vary from 0.2 ^{o}C/watt for a high power transistor to 1000 ^{o}C/watt for a low power transistor.

9. what is the condition for thermal stability?

Ans: Condition for thermal stability:

To avoid thermal runaway the required condition is that, the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated under steady state condition.

$$\text{i.e., } \frac{dP_C}{dT_J} < \frac{dP_D}{dT_J} \qquad \cdots\cdots \quad (1)$$

we know that, the steady state temperature rise at the collector junction is proportional to the power dissipated at the junction.

$$\text{i.e., } \Delta T = T_J - T_A = \theta P_D$$

where,

$T_J = junction\ temperature(^0C)$

$T_A = Ambient\ temperature(^0C)$

$P_D = Dissipated\ power\ at\ the\ collector\ junction(watts)$

$\theta = Thermal\ resistance$

$T_J - T_A = \theta P_D$

Differentiate with respect to T_J, we get,

$$\Rightarrow \quad 1 = \theta \frac{dP_D}{dT_J}$$

$$\Rightarrow \quad \frac{dP_D}{dT_J} = \frac{1}{\theta} \qquad \cdots\cdots (2)$$

Then, from equation (1), we have,

$\frac{dP_D}{dT_J} < \frac{1}{\theta}$ is the condition which must be satisfied to prevent thermal run away.

Thus, the transistor cannot runaway below a specified ambient temperature under any biasing condition.

10. Explain thermal instability. What are the factors affecting the stability factor?

Ans: Thermal instability:

The collector current for CE configuration is given by,

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$I_C = \frac{I_{CO}}{1-\alpha} + \frac{\alpha I_B}{1-\alpha}$$

i.e., change in temperature also effects the operating point i.e., I_{CO} doubles for every 10^0C rise in temperature.

The collector current causes the collector junction to rise its temperature. Hence, I_{CO} increases simultaneously and I_C also increases. This in turn increases the temperature and so I_{CO} still increases and then I_C. So, the transistor output characteristics will shift upwards. Then, the operating point changes. So, in certain cases, even if the operating point is fixed in the middle of active region, because of change in temperature, the operating point will be shifted to the saturation region.

The factors that affect the stability of Q point are

1) **I_{CO}:**

- The flow of current in circuit produces heat at the junctions. This heat increases the temperature at the junctions. We know that reverse saturation current I_{CO} increases with increasing temperature. Its value doubles for every 10^0C rise in temperature.
- Since $I_C = \beta I_B + (1+\beta) I_{CO}$
  The increase in I_{CO} increase the collector current I_C
- The increase in I_C further raises the temperature at the junction and the same cycle repeats.
- This excessive increase in I_C shifts the Q point into the saturation region, changing the operating condition set by biasing circuit.
- The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called ***thermal runaway***.

2) V_{BE}:

- V_{BE} changes with temperature at the rate of 2.5mV/ ^{0}C
- As I_B depends on V_{BE} and I_C depends on I_B [$since\ I_C = \beta I_B$], I_C depends on V_{BE}.
- Thus I_C changes with temperature due to change in V_{BE}. The change in collector current I_C change the operating point.

3) β:

- Since $I_C = \beta I_B$, as β varies, I_C also varies. The change in I_C change the operating point.

Problem1

Design the circuit shown in Fig. 6.24, given Q-point values are to be $I_{CQ} = 1$ mA and $V_{CEQ} = 6$ V. Assume that $V_{CC} = 10$ V, $\beta = 100$ and $V_{BE}\ (on) = 0.7$ V.

Solution: The collector resistance is

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{10 - 6}{1 \times 10^{-3}} = 4\ \text{k}\Omega$$

The base current is

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1 \times 10^{-3}}{100} = 10\ \mu\text{A}$$

The base resistance is

$$R_B = \frac{V_{CC} - V_{BE}\ (on)}{I_{BQ}} = \frac{10 - 0.7}{10 \times 10^{-6}} = 0.93\ \text{M}\Omega$$

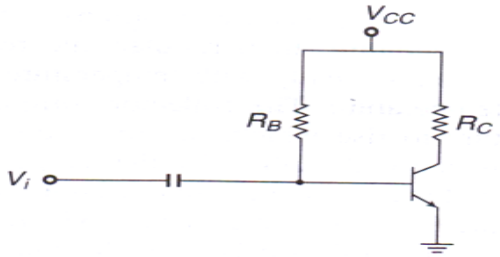


Fig. 6.24

Problem 2

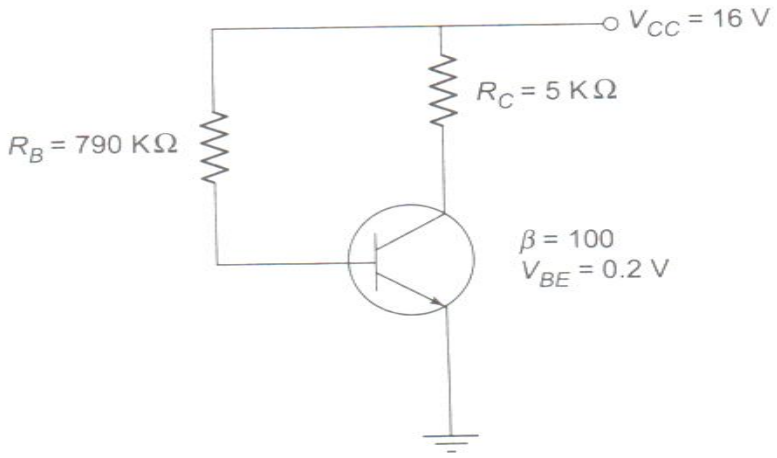
A Germanium transistor having $\beta = 100$ and $V_{BE} = 0.2\,V$ is used in a fixed bias amplifier circuit where $V_{CC} = 16\,V$, $R_C = 5\,k\Omega$ and $R_B = 790\,k\Omega$. Determine its operating point.

[JNTU Aug/Sep 2008]

Solution For a Germanium transistor, $V_{BE} = 0.2$ V

Applying KVL to the base circuit, we have

$$V_{CC} - I_B R_B - V_{BE} = 0$$



Therefore, $I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{16 - 0.2}{790 \times 10^3} = 20\,\mu A$

$I_C = \beta I_B = 100 \times 20\,\mu A = 2\,mA$

Applying KVL to the collector circuit, we have

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CE} = V_{CC} - I_C R_C = 16 - 2 \times 10^{-3} \times 5 \times 10^3 = 6\,V$

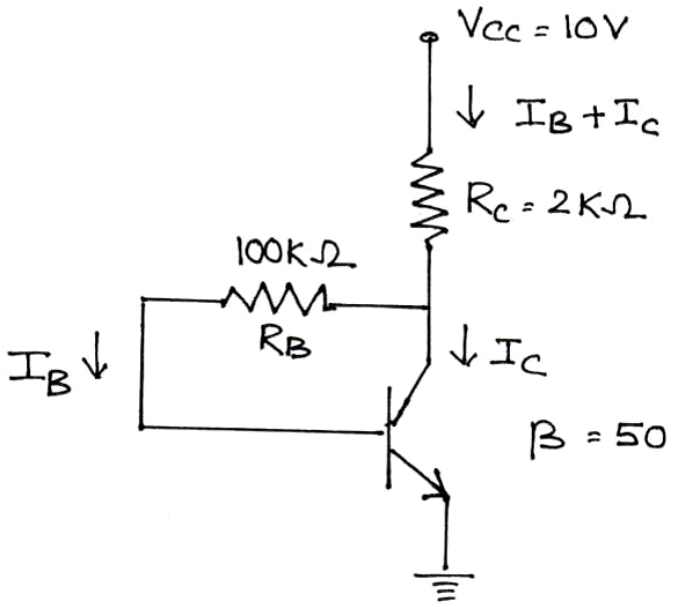
Hence, the operating point is $I_C = 2\,mA$ and $V_{CE} = 6\,V$.

Problem3

An N-P-N transistor with β=50 is used in a CE circuit with V_{CC}=10V, R_C=2KΩ. The bias is obtained by connecting a 100KΩ resistance from collector to base. Assume V_{BE}=0.7V. Find

i) the quiescent point and

ii) Stability factor 'S'



Solution:

i) Applying KVL to the base circuit

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$$

$$\Rightarrow V_{CC} = I_B (R_C + R_B) + I_C R_C + V_{BE}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \qquad \therefore I_C = \frac{\beta (V_{CC} - V_{BE} - I_C R_C)}{R_C + R_B}$$

$$\therefore I_C = \frac{50\left(10 - 0.7 - 2\times10^{-3} I_C\right)}{102\times10^3} \qquad \Rightarrow I_C = 2.3mA$$

Applying KVL to Collector Circuit

$$V_{CC} = \left(I_B + I_C\right) R_C + V_{CE} \qquad \therefore V_{CE} = V_{CC} - \left(I_B + I_C\right) R_C$$

$$= 10 - \left(46\times10^{-6} + 2.3\times10^{-3}\right)\times 2\times10^3$$

$$\Rightarrow V_{CE} = 5.308V$$ ∴ The quiescent point is **(5.308V, 2.3mA)**

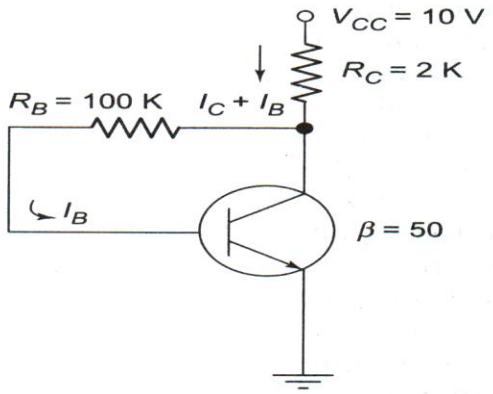
ii) Stability factor, S:

$$S = \frac{1+\beta}{1+\beta\dfrac{R_C}{R_C + R_B}}$$

$$\Rightarrow S = \frac{51}{1+50\left(\dfrac{20\times10^3}{102\times10^3}\right)} = 25.75$$

Problem4:

Calculate the quiescent current and voltage of collector to base bias arrangement using the following data: $V_{CC} = 10V,\ R_B = 100\ k\Omega,\ R_C = 2\ k\Omega,\ \beta = 50$ *and also specify a value of* R_B *so that* $V_{CE} = 7V$. *[JNTU May/June 2008]*



(a) Applying KVL to the base circuit, we have

$$V_{CC} - I_B(1+\beta)R_C - I_B R_B - V_{BE} = 0$$

Therefore, $I_B = \dfrac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C} = \dfrac{10 - 0.7}{100\times10^3 + (1+50)\times2\times10^3} = 46\ \mu A$

$$I_C = \beta I_B = 50\times46\ \mu A = 2.3\ mA$$

Applying KVL to the collector circuit, we have

$$V_{CC} - (I_B + I_C)R_C - V_{CE} = 0$$

Therefore, $V_{CE} = V_{CC} - (I_B + I_C)R_C$

$$= 10 - \left(46\times10^{-6} + 2.3\times10^{-3}\right)\times2\times10^3 = 5.308\ V$$

Quiescent current, $I_{CQ} = 2.3\ mA$ and

Quiescent voltage, $V_{CEQ} = 5.308\ V$

(b) Given $V_{CE} = 7\ \text{V}$

$$(I_B + I_C) R_C = V_{CC} - V_{CE}$$

$$(1+\beta) I_B R_C = V_{CC} - V_{CE}$$

$$I_B = \frac{V_{CC} - V_{CE}}{(1+\beta) R_C} = \frac{10-7}{(1+50)\times 2\times 10^3} = 29.41\ \mu\text{A}$$

We have,

$$V_{CC} = I_B R_B + V_{BE}$$

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{7-0.7}{29.41\times 10^{-6}} = 214.2\ \text{k}\Omega$$

Problem5

If the various parameters of a CE amplifier which uses the self bias method are $V_{CC} = 12\ V$, $R_1 = 10\ k\Omega$, $R_2 = 5\ k\Omega$, $R_C = 1\ k\Omega$, $R_E = 2\,k\Omega$ and $\beta = 100$, find

(a) the coordinates of the operating point and

(b) the stability factor, assuming the transistor to be silicon. *[JNTU 2008]*

Solution (a) *To find the coordinates of the operating point*

Refer to Fig. 4.16.

Thevenin's voltage, $V_T = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5\times 10^3}{15\times 10^3} \times 12 = 4\ \text{V}$

Thevenin's resistance, $R_B = \frac{R_1 R_2}{(R_1 + R_2)} = \frac{5\times 10^3 \times 10\times 10^3}{15\times 10^3} = 3.33\,\text{k}\Omega$

The loop equation around the basic circuit is

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

$$= \frac{I_C}{\beta} R_B + V_{BE} + \left(\frac{I_C}{\beta} + I_C\right) R_E$$

$$4 = \frac{I_C}{100} \times 3.33\times 10^3 + 0.7 + I_C \left(\frac{1}{100} + 1\right) \times 2\times 10^3$$

$$3.3 = (33.3 + 2020)\, I_C$$

$$I_C = \frac{3.3}{2053.3} = 1.61\,\text{mA}$$

Since I_B is very small, $I_C \approx I_E = 1.61\,\text{mA}$

Therefore, $V_{CE} = V_{CC} - I_C R_C - I_E R_E$

$$= V_{CC} - I_C [R_C + R_E] = 12 - 1.61 \times 10^{-3} \times 3 \times 10^3$$

$$= 7.17\ \text{V}$$

Therefore, the coordinates of the operating point are $I_C = 1.61\,\text{mA}$ and $V_{CE} = 7.17\ \text{V}$.

(b) *To find the stability factor S,*

$$S = (1+\beta)\frac{1 + \frac{R_B}{R_E}}{1 + \beta + \frac{R_B}{R_E}} = (1+100)\frac{1 + \frac{3.33\times 10^3}{2\times 10^3}}{1 + 100 + \frac{3.33\times 10^3}{2\times 10^3}} = 2.6$$

Problem6

In the circuit shown, if $I_C = 2$ mA and $V_{CE} = 3$ V, calculate R_1 and R_3 (Fig. 4.19).

[JNTU April/May 2007]

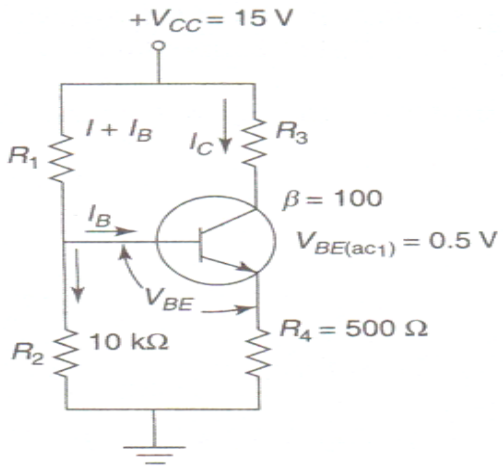


Fig. 4.19

Solution Given $\beta = 100, I_C = 2$ mA, $V_{CE} = 3$ V, $V_{BE} = 0.6$ V, $R_2 = 10$ kΩ and $R_4 = 500$ Ω

We know that $\beta = \dfrac{I_C}{I_B}$

Hence, $I_B = \dfrac{I_C}{\beta} = \dfrac{2\times10^{-3}}{100} = 20\ \mu A$

$$V_{CC} = I_C R_3 + V_{CE} + I_E R_4$$

$$I_E = I_C + I_B = 20 \times 10^{-6} + 2 \times 10^{-3} = 2.02 \text{ mA}$$

Substituting the values, we get

$$15 = 2 \times 10^{-3} \times R_3 + 3 \times 2.02 \times 10^{-3} \times 500$$

Therefore, $R_3 = 5.495$ kΩ

$$V_B = V_{BE} + I_E R_4 = 0.6 + 2.02 \times 10^{-3} \times 500 = 1.61$$

From the circuit, $V_B = \dfrac{R_2 V_{CC}}{R_1 + R_2}$

$$1.61 = \frac{10\times10^3 \times 15}{R_1 + 10\times10^3}$$

Therefore, $R_1 = 83.17$ kΩ

Amplifiers

1. Give the advantages of h-parameter analysis.

Ans: Analyzing the transistor circuits using h-parameters has the following advantages.

- The radio frequencies up to which, h-parameters are real numbers.
- h- parameters are very easy to measure.
- Using the transistor static characteristic curves, h-parameters can be found.
- In circuit analysis and design, these parameters are very convenient to use.
- h- parameters in one configuration can be easily converted into other configuration.
- These parameters are readily supplied by manufactures.

2. Analyze a single stage transistor amplifier using h-parameters.

Ans: Figure shows a single stage transistor amplifier with external load, signal source and proper biasing.

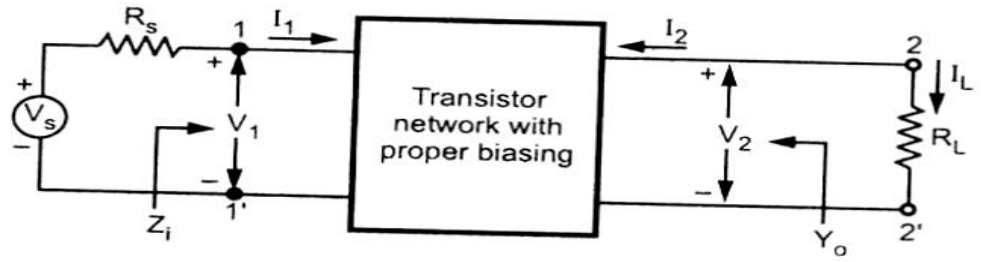


Fig: Basic amplifier circuit

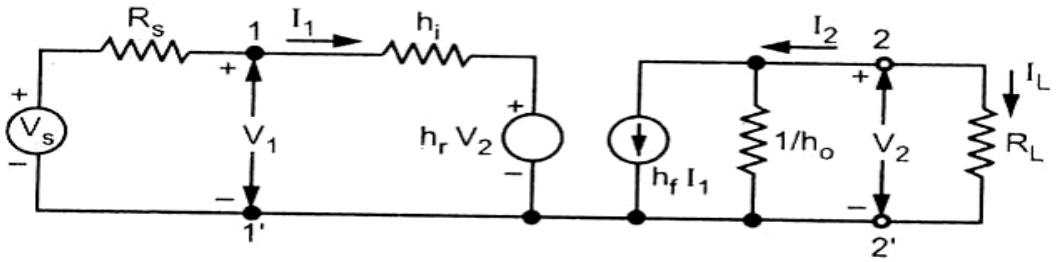


Fig: h-parameter equivalent circuit of the single stage transistor amplifier circuit.

Current Gain (or) Current Amplification, A_I

From output circuit $I_2 = h_f I_1 + h_0 V_2$

But $V_2 = I_L Z_L = -I_2 Z_L$

$\therefore I_2 = h_f I_1 - I_2 Z_L h_0$

$I_2 + I_2 Z_L h_0 = h_f I_1$

$I_2(1 + Z_L h_0) = h_f I_1$

$A_I = -\frac{I_2}{I_1} = \frac{-h_f}{1+Z_L h_0}$

$A_I = \frac{-h_f}{1+h_0 Z_L}$

Input Impedance (Z_i):

In the circuit, Rs is the signal source resistance. The impedance seen when looking into the amplifier terminals (1, 1') is the amplifier input impedance Z_i , i.e.,

$$Z_i = \frac{V_1}{I_1} = \frac{h_f I_1 + h_r V_2}{I_1} = h_f + \frac{h_r V_2}{I_1}$$

Substituting $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$Z_i = h_i + h_r A_I z_L$$

Substituting for A_I

$$Z_i = h_f - \frac{h_f h_r Z_L}{1 + h_o Z_L}$$

$$= h_i - \frac{h_f h_r}{Z_L\left[\frac{1}{Z_L} + h_O\right]} Z_L$$

Taking the load admittance as $Y_L = \frac{1}{Z_L}$

$$\therefore Z_i = h_i - \frac{h_f h_r}{Y_L + h_O}$$

Voltage Gain (or) Voltage Amplification factor (Av):

The ratio of the output voltage V_2 to the input voltage V_i gives the voltage gain of the transistor. i.e.,

$$A_V = \frac{V_2}{V_1}$$

Substituting $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i}$$

$$A_V = \frac{A_I Z_L}{Z_i}$$

Output Admittance (Y_O):

By definition, Y_O is obtained by setting V_1 to zero, Z_L to infinity and by driving the output terminals from a generator V_2. . If the current drawn from V_2 is I_2, then

$$Y_0 = \frac{I_2}{V_2} = with\ V_1 = 0\ \&\ R_L = \infty$$

From the circuit, $I_2 = h_f I_1 + h_O V_2$

Dividing by V_2, $\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_O$

From the circuit $V_1 = h_f I_1 + h_r V_2$

Dividing by V_2, & taking $V_1 = 0$

$$0 = h_f \frac{I_1}{V_2} + h_r$$

$$\Rightarrow \frac{I_1}{V_2} = \frac{-h_r}{h_f}$$

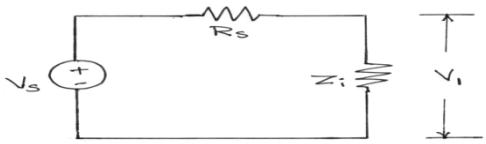
Using this equation in the above we get,

$$\frac{I_2}{V_2} = h_f \left(\frac{-h_r}{h_f}\right) + h_O$$

$$\therefore Y_O = h_o - \frac{h_f h_r}{h_i}$$

Voltage Amplification (A_{VS}) taking into account the resistance (R_S) of the source:

$$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} \times \frac{V_1}{V_s} = A_V \times \frac{V_1}{V_s}$$



$$V_1 = \frac{V_s Z_i}{Z_i + R_s}$$

$$\frac{V_1}{V_s} = \frac{Z_i}{Z_i + R_s} \; then \; A_{vs} = \frac{A_v Z_i}{Z_i + R_s}$$

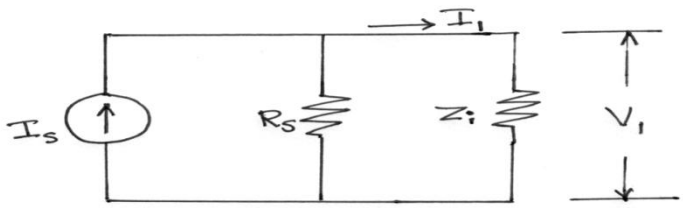
Substituting $A_v = \frac{A_I Z_L}{Z_i + R_s}$

Note that if $R_s = 0, then \; A_{vs} = \frac{A_I Z_L}{Z_i + R_s} = A_v$. Hence, A_V is the voltage gain with an ideal voltage source (with Rs=0). In practice, A_{VS} is more meaningful than A_V because source resistance has an appreciable effect on the overall amplification.

Current amplification (A_{IS}) taking into account the source resistance:

The equivalent input circuit using Norton's equivalent circuit for the source, for the calculation of A_{IS} is shown in fig. below.

Overall current gain, $A_{Is} = \frac{-I_2}{I_s} = \frac{-I_2}{I_1} \times \frac{I_1}{I_s} = A_I \times \frac{I_1}{I_s}$



$$I_1 = I_s \times \frac{R_s}{R_s + Z_i}$$

$$\frac{I_1}{I_s} = \frac{R_s}{R_s + Z_i}$$

If $R_S=\infty$, then $A_{IS} = A_I$. Hence, A_I is the current gain with an ideal current source (one with infinite source resistance).

$$\text{But}, \quad A_{vs} = \frac{A_I Z_L}{Z_i + R_s} \cdot \frac{R_s}{R_s}$$

$$\Rightarrow \quad A_{vs} = \frac{A_{IS} Z_L}{R_s}$$

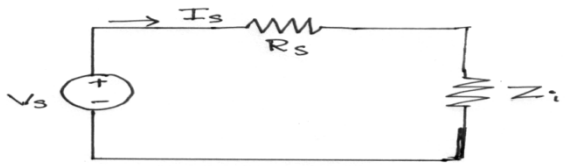
Power Gain:

$$A_P = \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_v A_I$$

$$A_P = A_I A_I \frac{R_L}{R_i}$$

$$\therefore A_P = A_I^2 \frac{R_L}{R_i}$$

Input impedance taking into account the source resistance (R_S):



$$Z_{is} = \frac{V_s}{I_s} = R_s + Z_I$$

$$\therefore Z_{is} = R_s + h_i + h_r A_I Z_L$$

Output impedance taking into account the source resistance (R_S):

By definition, Y_O is obtained by setting V_S to zero, Z_L to infinitely and by driving the output terminals from a generator V_2.

If the current drawn from V_2 is I_2, then $Y_0 = \frac{I_2}{V_2}$ *with* $V_s = 0$ & $R_L = \infty$

from the circuit, $I_2 = h_f I_1 + h_O V_2$

Dividing V_2, $\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_O$

With $V_s = 0$, by applying KVL input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$I_1(R_s + h_i) + h_r V_2 = 0$$

$$\therefore \frac{I_1}{V_2} = \frac{-h_r}{R_s + h_f}$$

Using this in the above equation, we get

$$\frac{I_2}{V_2} = h_f \left[\frac{-h_r}{R_s + h_i}\right] + h_O$$

$$\therefore Y_0 = h_0 - \frac{h_f h_r}{R_s + h_i}$$

3. Draw a circuit of the CE amplifier and explain its working.

Common Emitter Amplifier

Consider the transistor amplifier circuit shown in Fig.6.21. The emitter is common to both input and output. Hence this amplifier is known as common emitter amplifier. The resistors R_1, R_2 form the voltage divider network. The voltage drop across R_2 is used to bias the transistor. The coupling capacitor C_B is used to couple the input ac signal to the base of the transistor. It blocks any dc component present in the signal and passes only ac signal. The coupling capacitor C_C is used to couple the output signal to the next stage. The bypass capacitor C_E is connected in parallel with emitter resistance R_E to provide low reactance path to the ac signal. If C_E is not connected, the amplified ac signal passing through R_E will cause a voltage drop across it. This will reduce the output voltage and reduce the gain of the amplifier.

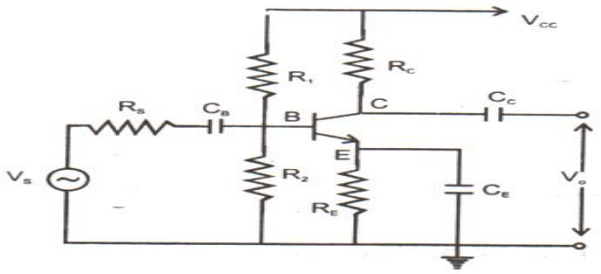


Fig. 6.21 Common emitter amplifier

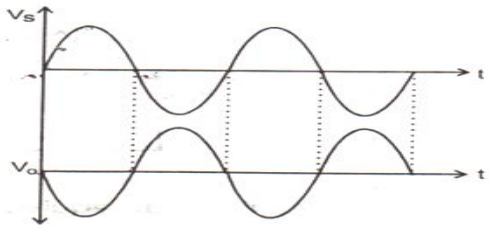


Fig. 6.22 Input and output voltage waveforms of an amplifier

The input and output voltage waveforms are shown in Fig.6.22. We can find that the output is 180° out of phase with input. This can be explained as follows. When the input is a positive going signal, the base current increases. This increase in base current increase collector current. When collector current is increased the drop across the resistor R_C increases and thus reducing level of the collector voltage. That is as input voltage is increased in a positive direction, the output V_o goes in negative direction. In the same way when the input waveform goes in negative direction, the base current decreases which decrease the voltage drop across R_C. This reduction, increase the output voltage level.

4. Draw a circuit of the CB amplifier and explain its working

Common Base (CB) Amplifier

Figure 9.33 shows the circuit of a single stage CB amplifier using an NPN transistor. The emitter-base junction is forward biased by power supply V_{EE}, whereas the collector-base junction is reverse biased by V_{CC}, so that the transistor remains in the active region throughout its operation.

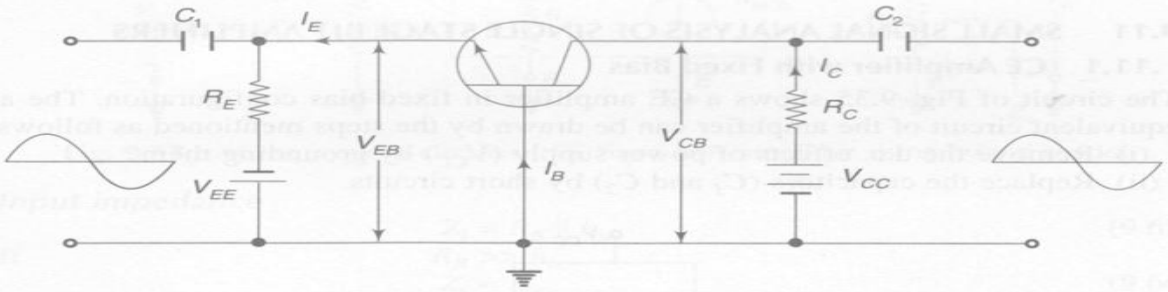


Fig. 9.33 Common base amplifier

Input signal applied to the emitter-base circuit and output signal is taken from collector-base circuit. The output voltage ($= V_{CB}$) is given by the equation

$$V_o = V_{CC} - I_C R_C \qquad (9.64)$$

When a sinusoidal a.c. signal is applied at the input, during the positive half cycle of the applied signal, the amount of forward bias to base-emitter junction is decreased, resulting in a decrease in I_B. As a result I_E ($\approx \beta I_B$) and hence, I_C also decreases.

From Eqn. (9.64), the drop $I_C R_C$ decreases, hence $V_o = V_{CB}$ correspondingly increases. Thus, a positive half cycle appears at the output without any phase reversal as shown in Fig. 9.34.

5. Draw a circuit of the CC amplifier and explain its working

Common Collector Amplifier (Emitter follower)

Fig.6.32 shows the circuit diagram of a common collector amplifier. This circuit diagram is also known as emitter follower because its voltage gain is close to unity. Hence a change in base voltage appears as an equal change across the load. The input impedance of a common collector amplifier is high and the output impedance is low. Hence it is used as a buffer or impedance matching network that transfers maximum power between the source and load. In addition, the common collector amplifier increases the power level of the signal. The *ac* equivalent circuit is shown in Fig.6.33 and the h-parameter model of CC amplifier is shown in Fig.6.34. Here we assumed h_{re} is very small.

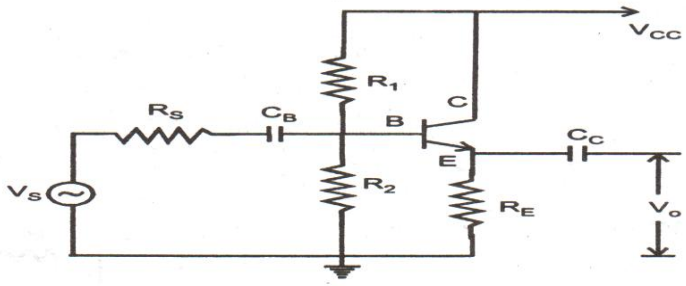
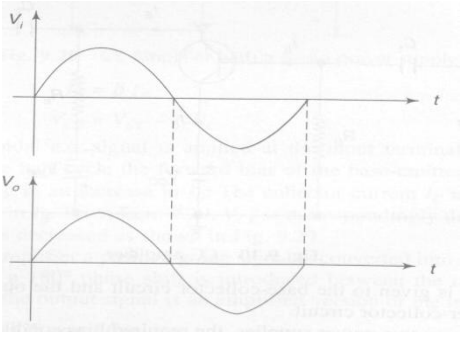


Fig. 6.32 Common collector amplifier



Example Problem 6.4 **[May/June - 08]**

The h-parameters of a transistor used in a CE circuit are h_{ie} = 1.0 kΩ, h_{re} = 10 × 10^{-4}, h_{fe} = 50, h_{oe} = 100 μA/V. The load resistance for the transistor is 1 kΩ in the collector circuit. Determine Z_i, A_v and A_i in the amplifier stage (Assume R_s = 1000Ω)

Sol. :

Current gain,

$$A_I = \frac{-h_{fe}}{1 + h_{oe}R_L}$$

$$= \frac{-50}{1 + 100 \times 10^{-6} \times 10^3}$$

$$= -45.45$$

Input impedance

$$Z_i = h_{ie} + h_{re}A_IR_L$$

$$= 1 \times 10^3 + 10 \times 10^{-4} \times -45.45 \times 10^3$$

$$= 1000 - 45.45 = 954.55\ \Omega$$

Voltage gain,

$$A_V = \frac{A_IR_L}{Z_i}$$

$$= \frac{(-45.45)(1 \times 10^3)}{954.55} = -47.61$$

Output admittance,

$$Y_o = h_{oe} - \frac{h_{fe}h_{re}}{h_{ie} + R_s}$$

$$= 100 \times 10^{-6} - \frac{50 \times 10 \times 10^{-4}}{10^3 + 10^3}$$

$$= 100 \times 10^{-6} - 25 \times 10^{-6}$$

$$= 75 \times 10^{-6}$$

$$= 75\ \mu A/V\ (or)\ 75\ \mu\mho$$

Output Impedance

$$Z_o = \frac{1}{Y_o}$$

$$= \frac{1}{40} = \frac{1}{75 \times 10^{-6}} = 13.33\ k\Omega$$

Short Questions and Answers

1. **Define valence electron.**

   Electrons that are in shells close to nucleus are tightly bounded to the atom and have low energy, whereas the electrons that are in shells farther from the nucleus have large energy and less tightly bound to the atom. Electrons with highest energy level exist in the outermost shell of an atom. These electrons determine the electrical and chemical characteristics of each particular type of atom. These electrons are known as valence electrons.

2. **What is meant by energy band?**

   In a single isolated atom, the electron in any orbit possesses definite energy. Due to an interaction between atoms the electrons in the particular orbit of one atom have slightly different energy levels from electrons in the same orbit of an adjoining atom. This is due to the fact that no two electrons see exactly the same pattern of surrounding charges. Since there are billions of electrons in any orbit, slightly different energy levels form a cluster or band known as energy band.

3. **Define conduction band.**

   The conduction band is defined as the range of energies possessed by conduction electrons.

4. **Define valence band.**

   The valence band is defined as the range of energies possessed by valence electrons.

5. **What are conductors, Insulators and semiconductors?**

   A conductor is a material, which easily allow the flow of electric current. The best conductors are copper, silver, gold and aluminum.

   An insulator is a material that does not conduct electric current. In these metals valence electrons are tightly bound to the atoms.

   A semiconductor is a material that has electrical conductivity that lies between conductors and insulators. A semiconductor in its pure state is neither a good conductor nor a good insulator. The most common semiconductors are silicon, Germanium, and carbon.

6. **What are the classifications of semiconductors?**

   The semiconductors are classified as intrinsic and extrinsic semiconductors. A pure semiconductor is called intrinsic semiconductor. A doped semiconductor is called as an extrinsic semiconductor.

7. **What is meant by doping?**

   The process of adding impurities to a semiconductor is known as doping.

8. **How the extrinsic semiconductors are classified?**

   (a) n-type semiconductor

   (b) p-type semi conductor

9. **How the n-type semiconductor can be obtained?**

   The n-type semi conductor can be obtained by adding pentavalent impurities to intrinsic semiconductor. These are atoms with five valence electrons. Typical examples for pentavalent atoms are Arsenic, Phosphorous, bismuth and antimony.

10. **How the p-type semiconductor can be obtained?**

    The p-type semi conductor can be obtained by adding trivalent impurities to intrinsic semiconductor. These are atoms three valence electrons. Typical examples for trivalent atoms are boron (B), indium (In) and gallium (Ga)

11. **Define i) mean free path ii) mean free time.**

    The average distance traveled by an electron between collisions is called the mean free path and the average time between collisions is called its mean free time.

12. **Define Fermi level.**

    Fermi level is the energy at which the probability of occupation by an electron is exactly 0.5.

13. **What is Fermi-Dirac distribution function?**

    The probability that electronic state with energy E is occupied by an electron is given by the Fermi - dirac distribution function.

$$f(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

where k = Boltzmann's constant
E_F = Fermi energy level
T = absolute temperature in $^\circ K$

14. **For intrinsic semi conductor where the Fermi level lies?**

    The Fermi level lies in the center of the forbidden energy band for an intrinsic semiconductor.

15. **What is energy band gap of silicon and Germanium at $300^\circ K$?**

    For Germanium 0.66eV
    For Silicon 1.12e V

16. **For a p-type semiconductor where the Fermi level lies?**

For a p-type semiconductor the Fermi level lies just above valence band

17. **For a n-type semiconductor where the Fermi level lies?**

For a n-type semiconductor the Fermi level lies just below conduction band.

18. **What is mass action law?**

Under thermal equilibrium the product of number of holes and the number of electron is constant and is independent of the amount of donor and acceptor atoms. This relation is known as mass-action law and is given by

$$np = n_i^2$$

19. **Define energy gap. How it varies with temperature?**

The energy gap is equal to the difference of energy levels between the conduction band and valence band of the semiconductor crystal structure and it is the energy required to break a covalent bond. The energy gap at any temperature (T) in Kelvin is expressed by the relation

$$E_G = E_{GO} - \frac{\alpha T^2}{(T+\beta)} \tag{2.203}$$

20. **Write an expression for the conductivity of a semiconductor.**

The conductivity of a semiconductor is given by

$$\text{Where} \qquad \sigma = (n\mu_n + p\mu_p)q$$

21. **What is Einstein's relation?**

At a fixed temperature, the ratio of diffusion constant to the mobility is constant. Mathematically it is expressed as

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = kT \tag{2.204}$$

22. **Define volt equivalent temperature**

Volt equivalent temperature is the product of kT where k is Boltzmann's constant expressed in $eV/^\circ K$.

$$V_T = kT$$

If k is expressed in Joules /°K then $V_T = \overline{k}T/q$

23. **Write continuity equation.**

The continuity equation is given by

$$\frac{\partial_P}{\partial t} = \frac{p_o - p}{\tau_p} - \frac{1}{q}\frac{\partial J_p}{\partial_x} \tag{2.205}$$

24. **How the pn junction is formed?**

The pn junction diode formed by two blocks of semiconductor material; one of p-type material and the other of n-type material.

25. **What is depletion region?**

When the pn junction is formed free electrons from the n-side diffuse across the junction, and fill holes on the p side and create positive ions. Similarly the holes from p-side diffuse across the junction and recombine with electrons in n-side and create negative ions. Since negative ions are created on p-side of the junction, the region close to the junction acquire a negative charge. Similarly the positive ions created on the n-side gives a positive charge near the junction. As these charges built up a point is reached where the total negative charge in p-region repels any further diffusion of electrons (negatively charge particles) into the p-region (like charges repels) and the diffusion stops. At this point the positive ions on n-side and negative ions on p-side are immobile (fixed). They cannot serve as current carriers. That is the region is almost completely depleted of carriers. This region near the junction is called the depletion region. The width of the depletion region is about $1\mu m(10^{-6}m)$.

26. **What is barrier potential?**

The intimate contact between p and n materials form a depletion layer near the junction. Since the depletion layer contains positive charges on one right side of the pn junction and negative ions on the left side of the pn-junction an electric field is formed. The electric field produce a barrier to the flow free electrons in the n-region, and energy must spend to move an electron through the electric field. That is an external energy must be applied to move an electron through the electric field. The external energy depends on the potential difference of the electric field across the depletion region. This potential difference which is required to move electrons through the electric field is known as barrier potential (V_o) and it is expressed in volts.

27. **What is the barrier potential for Ge and Si?**

The barrier potential for GE is 0.3 V and for Si 0.7V

28. **What is meant by forward bias?**

When the positive terminal of the battery is connected to p-side of the device and the negative terminal is connected to n-side of the device then the device is said to be forward biased.

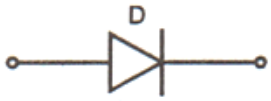
29. **What is meant by reverse bias?**

When the negative terminal of the battery is connected to p-side and positive terminal is connected to n-side then the device is said to be reversed biased.

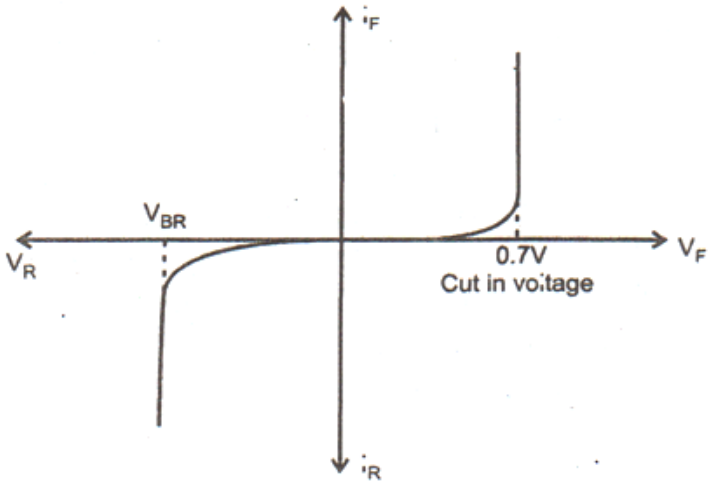
30. **What is meant by break down voltage?**

If the reverse bias voltage is increased, the velocity of minority charge carriers crossing the junction increases. These carriers acquire high kinetic energy and collide with atom. As a result the valence electron in the atom observes sufficient energy and leave the parent atom. These additional carriers also get sufficient energy from the applied reverse bias and collide with other atoms and generate some more carriers. This collision and generation of carriers is a cumulative effect, which result in large amount of reverse current. This phenomena, known as reverse breakdown occurs at a particular reverse voltage for a *pn* junction. This voltage is known as reverse breakdown voltage.

31. **Draw the symbol of a diode**



32. **Draw the V-I characteristics of a diode.**



33. **Define static and dynamic resistances of a diode.**

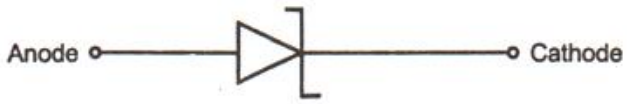
The static resistance R_F of a diode is defined as the ratio V/I of the voltage to the current can be obtained by finding the reciprocal of the slope of a line joining the operating point to the origin. But it is not a useful parameter as the resistance varies widely with V and I. The dynamic resistance r_f is defined as the reciprocal of the slope of volt-ampere characteristics.

$$r_f = dV/dI$$

34. **What are the applications of a diode?**

In rectification, clampers, clippers, switching circuits, comparators,voltage doublers and diode gates

35. **Draw the symbol of zener diode.**



36. **In what region of the V - I characteristics, the zener diode is operated?**

The zener diode is a pn junction device that is designed to operate in reverse breakdown region.

37. **How much voltage appears across a zener diode when it is forward biased?**

For silicon diode the voltage is 0.7 V
For germanium diode the voltage is 0.3V.

38. **How the breakdown voltage of a zener diode is set during manufacturing.**

The breakdown voltage of a zener diode is set by controlling the doping level during manufacturing.

39. **What is avalanche breakdown?**

When pn junction is reversed biased, the minority carriers constitute the flow of reverse saturation current through the diode. These carriers acquire energy from applied potential and collide with crystal ion. This collision generates an electron-hole pair. The additional pair generated acquire sufficient energy and generates another electron-hole pair, by collision. Thus each new charge carrier in turn produce additional charge carriers by breaking covalent bonds. As a result the number of charge carriers avalanches and results in break down.

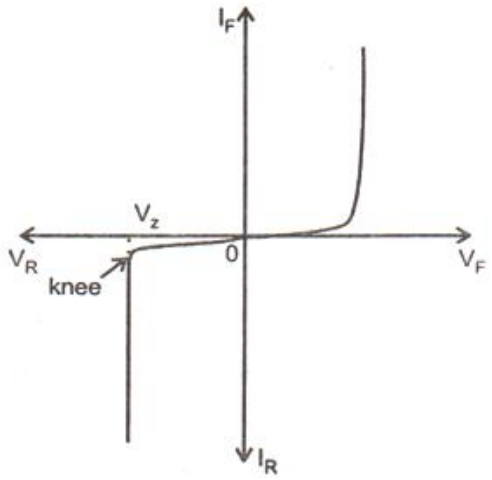
40. **What is mean by Zener breakdown?**

When the p and n - regions are heavily doped, the width of the depletion region becomes very small. As a result, a small voltage (around 5V) can produce high electric field intensity with in narrow depletion region. Recall that

$$\text{Electric field intensity} = \frac{\text{Reverse voltage}}{\text{Width of depletion layer}}$$

Under the influence of high electric field intensity direct rupture of covalent bonds take place. The new electron - hole pairs thus created increase the reverse saturation current.

41. **Plot the V-I characteristics of a zener diode.**



42. **What are the different types of voltage regulators?**

Based on how regulating element is connected to the load, the voltage regulators are classified as

i) Series regulator

ii) Shunt regulator

43. **What are applications of the zener diode?**

Zener diodes are used as voltage regulator and voltage limiters.

44. **Describe tunnelling phenomenon.**

When the doping level is increased the depletion region reduces. Due to thin depletion region, even for very small forward bias many carries penetrate through the junction and appear at the other side. This phenomenon of penetration of carriers through the depletion region is known as tunnelling.

45. **What are the key characteristics of a tunnel diode?**

The key characteristics of a tunnel diode is its negative resistance region.

46. **What are the applications of tunnel diode?**

i) Relaxation oscillator

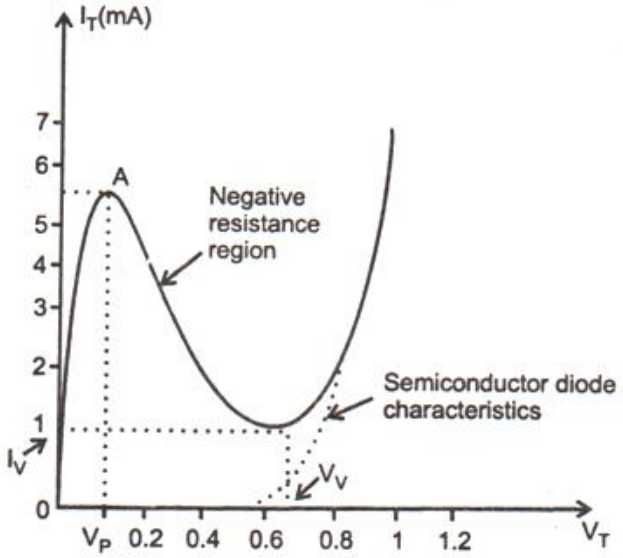
ii) Micro wave oscillator

iii) Storage device

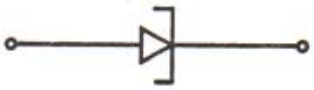
iv) Pulse generator

v) High speed switching networks

47. **Draw the V-I characteristics of tunnel diode.**



48. **Draw the symbol of tunnel diode.**



49. **What are the advantages and disadvantages of tunnel diode?**

Advantages:

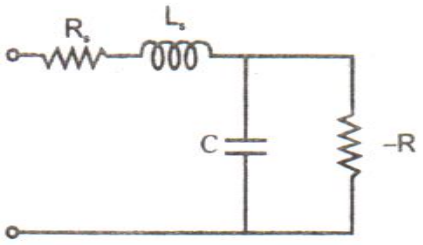
Low cost, low noise, high speed, and low power consumption.

Disadvantages:

i) Low output voltage swing

ii) No isolation between input and output.

50. **Draw the equivalent circuit of tunnel diode.**



51. **What is the difference between backward diode and tunnel diode?**

The backward diode is a tunnel diode with suppressed I_p.

52. **What is the difference between backward diode and zener diode?**

For a backward diode the reverse breakdown voltage is less than that of the zener reverse breakdown voltage.

53. **What is the main application of backward diode?**

Backward diodes are used to rectify weak signals whose peak amplitudes are between 0.1V and 0.7V.

54.

Draw the symbol of varactor diode.

57. **Explain how a reverse biased pn junction exhibits a capacitor?**

The width of the depletion layer can be controlled using reverse bias voltage. Since the depletion layer is an insulator, the pn junction can be thought of a parallel plate capacitor, the p and n regions acts like plates of a capacitor (p-region positive plate, n-region negative plate).

58. **Discuss how the capacitance varies with reverse bias voltage.**

The depletion region increases as reverse voltage applied to diode increases. Since capacitance varies inversely with dielectric thickness $\left(C_T = \frac{\varepsilon A}{w}\right.$; as w increases c decreases$\left.\right)$, the junction capacitance will decrease as the voltage across pn junction increase.

59. **Varactor diode operates in forward bias condition True / False.**

False

60. **What are the applications of varactor diode?**

i) Varactor diode is used in TV Receiver, AFC Circuits, adjustable band pass filters.

ii) In frequency modulators.

iii) Used in phase locked loop (PLL) & frequency locked loop (FLL)

iv) Very low noise microwave parametric amplifiers.

What is the principle of working of LED?

It works based on electroluminescence a process that changes an electric input to a light output, the opposite of the photovoltaic effect.

What materials are used to construct a LED?

Gallium arsenide ($GaAs$)
Gallium Phosphide (GaP)
Gallium arsenide Phosphide ($GaAsp$)
Aluminium gallium arsenide ($AlGaAs$)

61.

What are the applications of LED?

i) LEDs are more popularly used in displays clocks, audio and video equipments, traffic lights.

ii) It is also used as light source in optical fiber communication.

1. **What is a *dc* power supply? What are its basic elements?** The *dc* power supply converts the *ac*voltage. It consists of the following elements. The transformer, rectifier, filter and voltage regulator.

2. **What is the function *dc* regulator in *dc* power supply?**

   The function of regulation is to keep the *dc* voltage constant in spite of load and input voltage variations.

3. **What is a rectifier?**

   A rectifier is a wave shaping circuit that converts *ac* voltage to *dc* voltage.

4. **Define voltage regulation.**

   The degree to which the *dc* output voltage changes under load conditions is measured by voltage regulation. It is defined as the variation of the *dc* output voltage as a function of the *dc* current.

$$\% \quad \text{regulation} = \frac{V_{\text{no load}} - V_{\text{full load}}}{V_{\text{full load}}}$$

5. **Define efficiency of a rectifier.**

   The efficiency η of a rectifier is defined by the ratio

$$\eta = \frac{dc \text{ power supplied to the load}}{\text{Total input } ac \text{ power}} \times 100$$

6. **Define ripple factor.**

   The ripple factor is a measure of how successful a rectifier converts *ac* to *dc*. It is the ratio of *rms* value of *ac* component to the dc value.

$$\text{Ripple factor} = \frac{V_{r(rms)}}{V_{dc}}$$

7. **Define form factor.**

The form factor is defined as the ratio of rms value of the laod voltage to the *dc* component. Form factor = $\frac{V_{rms}}{V_{dc}}$

8. **Define Peak Inverse Voltage (PIV)**

The secondary voltage that appear across the diode when it is reverse biased is called peak inverse voltage (PIV)

9. **Define transformer utilization factor.**

The transformer utilization factor is defined as

$$\text{Transformer utilization factor} = \frac{dc \text{ power delivered to the load}}{ac \text{ rating of the transformer secondary}}$$

10. **What are the advantages and disadvantages of fullwave rectifier?.**

Advantages

(a) The efficiency is high.
(b) Higher TUF and better voltage regulation.
(c) The *dc* saturation of the core is avoided as current flows through the two halves of the center tapped secondary in both directions.
(d) Low ripple factor.

Disadvantages

(a) Need center tapped transformer which is bulky and cost.
(b) Diodes with high PIV rating are needed.

11. **What are the advantages and disadvantages of bridge rectifier?**

Advantages of Bridge rectifier

(a) The efficiency is high
(b) The ripple factor is low
(c) High TUF
(d) Does not require a center tapped transformer
(e) The PIV rating of diode is only V_m
(f) No desaturation of the core.

Disadvantage

Require four dio des.

1. **What is a transistor? Why this electronic device is aptly named?**

   In basic amplifying action of a transistor the signal is transferred from a low resistance to a high resistance. Hence the combination of two terms Transfer+resistor→transistor is named to the device.

2. **Describe the basic structure of the BJT.**

   Bipolar junction transistor (BJT) is a three-layer semiconductor device consisting of two *PN* junctions. If a layer of n-type material is sandwitched between two layers of p-type, the transistor is known as *pnp* transistor. On the other hand if a layer of p-type material is sandwitched between two layers of n - type, the transistor is known as *npn* transistor.

3. **What are the three terminals in a BJT?**

   (a) Emitter (E)

   (b) Collector (C)

   (c) Base (B)

4. **What are the bias conditions of the base-emitter and base-collector junction for a transistor to operate as an amplifier?**

   The transits operate as an amplifier when the base-emitter junction is in forward bias condition and base-collector junction is in reverse bias condition.

5. **If the collector current is 2mA and the base current is 25μA. What is the emitter current?**

   Solution

   Given $I_C = 2mA$

   $I_B = 25\mu A$

   We know that $I_E = I_B + I_C$

   $= 2mA + 25\mu A$

   $I_E = 2.025\ mA$

6. **Define dc beta.**

   The dc beta (β_{dc}) is defined as the ratio between the collector current (I_C) to the base current (I_B). If is also known as common emitter current gain.

$$\beta_{dc} \simeq \frac{I_C}{I_B}$$

7. **Define dc alpha.**

The dc alpha (α_{dc}) is defined as the ratio between the collector current (I_C) to emitter current (I_E). It is also known as common base current gain.

$$\alpha_{dc} \simeq \frac{I_C}{I_E}$$

8. **What are the bias condition of the base-emitter and collector-base junction to operate transistor in cut-off region?**

The transistor operate in cut-off region if the base-emitter junction and collector base junction are reversed biased.

9. **If $\alpha_{dc} = 0.98$, what is β_{dc}.**

Solution

$$\text{Given} \quad \alpha_{dc} = 0.98$$

$$\text{we know that} \quad \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}$$

$$= \frac{0.98}{1 - 0.98} = \frac{0.98}{0.02} = 49$$

$$\beta_{dc} = 49$$

10. **Why is silicon preferred over germanium in the manufacture of semiconductor devices?**

As the knee voltage of silicon is higher (0.7v) than the knee voltage of germanium (0.3v) silicon will be stable for temperature variation than germanium.

11. **Deduce the relationship between α and β**

$$\beta = \frac{\alpha}{1 - \alpha}$$

12. **Which amplifier has lowest input impedance?**

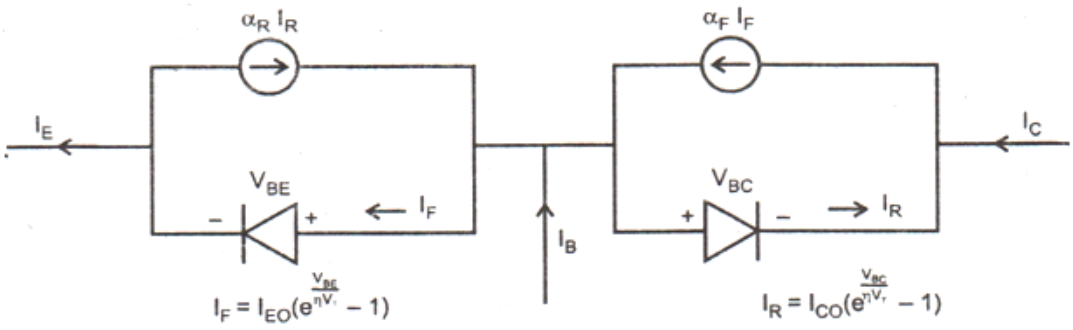
Common base amplifier has a lowest input impedance

13. **Describe how amplification and switching are achieved by a BJT?**

For amplification, BJT must operate in the active region.

For switching, cut - off and saturation regions of output characteristics are used. When it is saturated, it acts as a closed switch. When it is in cut-off stat it acts as on open switch.

14. **Draw the Ebers-moll model of a transistor.**



15. **What is early effect?**

In the active region of a common-base transistor, the emitter junction is forward biased and the collector junction is reversed biased. When the reverse bias applied to collector junction increased the depletion region at the collector junction increases. Since the base is lightly doped when compared to collector, the depletion region penetrates deeply into the base of the transistor. Since the penetration of the depletion region into base is much large than into the collector, collector depletion region is neglected. If the actual base width is W_B and the width of the depletion region is W then effective electrical base width is $W_B = W_B - W$. This depenendency of base width on the applied reverse bias to collector voltage is known as early effect.

16. **What is the other name for early effect?**

Since base width is varying with increasing in reverse collector voltage the early effect alsc known as base width modulation.

17. **What are the different ways of transistor breakdown?**

There are two different ways of transistor breakdowns are possible.

(a) Avalanche Multiplication

(b) Punch-through (or) reach-through

18. **What is meant by punch through?**

We know that the depletion region increases with increasing reverses bias. Since the base is highly doped depletion region, penetrates deeper into base and the undepleted part of the base becomes narrow. If the reverse bias is increased further a stage is reached at which the depletion region spread completely across to the emitter junction, this phenomenon is know as reach - through.

19. **Explain about avalanche multiplication.**

The breakdown mechanism of BJT is similar to that *pn* junction diode. Since the base - collector junction is reverse biased; it is the junction where breakdown occurs. Avalanche breakdown is caused by impact ionization. Electron hole pair is generated in the collector because of the high kinetic energy. These holes are forced to the base by the electrical field including an electron current $\beta_M I_C$ where M is the avalanche multiplication factor $\beta_M > 1$ results in avalanche an unlimited increases in the collector current without any further external control. This causes the BJT to breakdown.

20. **What are the features of JFET?**

(a) The operation of FET depends upon the flows of majority carriers only.

(b) The input impedance of FET is very high, in the order of $M\Omega$.

(c) The FET is less noisy than BJT.

(d) It exhibits no offset voltage at zero drain current.

(e) It is simple to fabricate.

(f) It occupies less space in integrated circuit.

21. **What are the different types of FET.**

(a) Junction Field Effect Transistor (JFET).

(b) Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

22. **Define amplification factor.**

The amplification factor (μ) is defined as the ratio between change in drain-source voltage (V_{DS}) and change in gate - source (V_{GS}) at constant drain current (I_D).

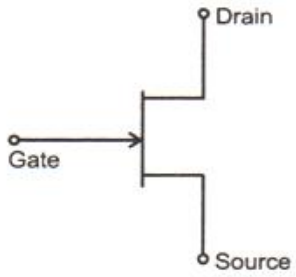
$$\mu = \left.\frac{\partial V_{DS}}{\partial V_{GS}}\right|_{I_D}$$

23. **Define transconductance (g_m)**

The transconductance (or) mutual conductance is defined as the ratio between change in drain current (i_D) and change in gate - source voltage (V_{GS}) at constant drain - source voltage (V_{DS}).

$$g_m = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}}$$

24. **Draw the symbol of JFET.**



25. **Define drain resistance.**

The drain resistance or output resistance (r_d) is defined as the ratio between change in drain - source voltage (V_{DS}) and change in drain current (I_D) at constant gate - source voltage (V_{GS}).

$$r_d = \left.\frac{\partial V_{DS}}{\partial i_D}\right|_{V_{GS}}$$

26. **What is mean by pinch-off voltage?**

Pinch - off voltage (V_P) is defined as the drain to source voltage above which drain current becomes almost constant.

27. **What is I_{DSS} in JFET?**

The drain to source voltage at which pinch-off occurs is known as pinch-off voltage V_P and corresponding I_D is known as I_{DSS}.

28. **Write Shockley's equation.**

The relation between V_{GS} and I_D can be represented by Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Where I_{DSS} = Maximum value of drain current when $V_{GS} = 0$

V_p = pinch-off voltage.

29. **What are the different types of MOSFET?**

The modes of operation of the MOSFET are divided in to two types.

(a) Depletion mode MOSFET
(b) Enhancement mode MOSFET

30. **What is the other name for MOSFET?**

Metal oxide semiconductor field effect transistor (MOSFET) is also called as insulated gate field effect transistor (IGFET)

31. **What are the application of JFET?**

(a) FET is used as a buffer in measuring instruments since it has high input impedance and low output impedance.

(b) FET is used in RF amplifier in FM tuners and communication equipment.

(c) FET is used in digital circuit in computers and memory circuit because of its small size.

(d) It is used in oscillators because frequency drift is low.

32. **If the gate-to-source voltage in a enhancement MOSFET is zero, what is the current from drain to source?**

In an enhancement MOSFET the gate-to-source voltage is zero, then the current from drain to source is also zero ($I_o \simeq 0$).

33. **What is the major difference in construction of the D - MOSFET and the E - MOSFET?**

The depletion MOSFET has a structural channel, the enhancement - MOSFET does not.

34. **If the gate-to-source voltage in a depletion MOSFET is zero, what is the current from drain-to-source?**

When gate - source voltage is zero for depletion MOSFET, the drain - source current is equal to I_{DSS}. ($I_D \simeq I_{DSS}$)

35. **What are the precautions to be taken when handling MOSFET?**

(a) MOSFET should be shipped and stored in conduction foam rubber.
(b) Prior to soldering, the technician should use a shorting strap to discharge his static electricity.
(c) The soldering iron tip to be grounded.
(d) MOSFETs should never be inserted into or remove from a circuit with the power on.
(e) The assembler should wear antistatic clothes and ground wrist beads.
(f) All the instruments and metal benches used to test the MOS devices should be connected to ground.

36. **What are the differences between BJT and JFET?**

Bipolar junction transistor BJT	Junction field effect transistor JFET
Bipolar device (current conduction is by both electrons and holes)	Unipolar device (current is by only one type of carrier either electrons or holes)
Low input impedance due to forward bias	High input impedance due to reverse bias
Current control device	Voltage control device
Gain is characterized by voltage gain	Gain is characterized by transconductance.
High noise level	Low noise level.

37. **What are the differences between JFET and MOSFET?**

JFET	MOSFET
Reverse bias for gate	Positive or negative gate voltage
Gate is formed as a diode	Gate is formed as a capacitor
Operated only in depletion mode	Can be operated either in depletion mode or in enhancement mode.
High input impedance	Very high input impedance due to capacitive effect.

38. **Write down the relationship between various FET parameters?**

$$\text{Amplification factor} = \text{Drain resistance} \times \text{Transconductance}$$

$$\mu = r_d \times g_m$$

39. **What are the applications of MOSFET?**

(a) It can be used as input amplifiers in oscilloscopes, electronics voltmeters etc.

(b) It is used in logic circuits.

(c) It is used in computer memories.

(d) It is used in phase shift oscillators.

(e) It is used in FM and TV receivers.

40. Depletion MOSFET is commonly known as "Normally-on" MOSFET why?

The depletion MOSFET can conduct even if the gate to source voltage (V_{GS}) is zero. Because of this reason depletion MOSFET is commonly known as normally on MOSFET.

41. What are the parametcrs of JFET?

There are three parameters of JFET, they are

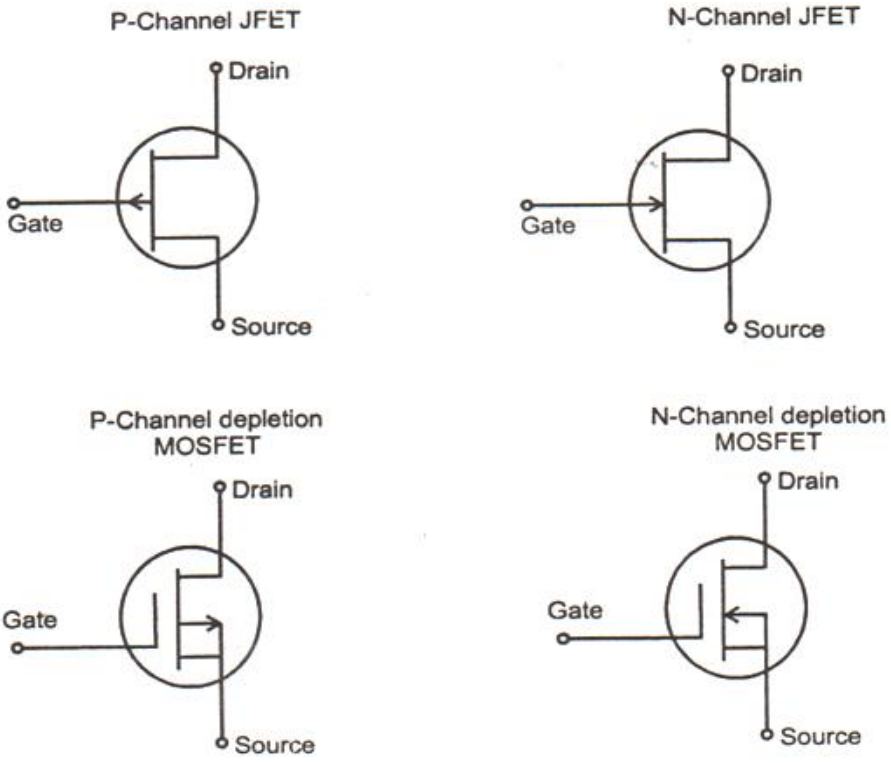
(a) ac drain resistance (r_d)

(b) Transconductance (g_m)

(c) Current amplification factor (μ).

42. Draw the symbol of the following.

(i) P - channel JFET (ii) N - channel JFET
(iii) P - channel depletion MOSFET (iv) N - channel depletion



1. **What is meant by amplification? Define faithful amplification.**

   The process of converting weak signal in to strong signal is called amplification. After amplification if the shape of the output signal is same as the input signal then the amplification is said to be faithful amplification. That is after amplification the shape of the output signal must be same as input with increase in magnitude.

2. **In what region of the characteristics the transistor is operated amplifier?**

   Active region

3. **Define operating point (or) Define quiescent point.**

   The operating point is the values of I_C and V_{CE} when there is no input signal at the base terminal.

4. **What are the effects on the output signal if the operating point is not properly chosen?**

   If the operating point is not properly chosen then the transistor may drive into saturation or cutoff during input voltage swing. As a result the output of the amplifier is clipped. In this case the output is said to be distorted.

5. **What are the factors that affect the stability of operating point?**

   The factors that affect the stability of operating point are

   (a) ~~Temperature~~ I_{CO} (c) V_{BE}

   (b) β of the transistor.

6. **What is the effect of change in temperature on the stability of operating point?**

   The reverse saturation current doubles for every $10°C$ rise in temperature. Since

   $$I_C = \beta I_b + (1 + \beta) I_{co}$$

   the increase in I_{co} increase the collector current I_C which in turn increase the collector-junction temperature. As a result I_{co} increases which further increase I_C. That is if the temperature is increased then the collector current also increase shifting the operating point upwards. Now the operating point is close to saturation than before. If we apply the input signal, the transistor may drive into saturation during positive cycle of the input signal. The could cause clipping and bad distortion in the output.

7. **Define Stability factor.**

The extent to which the stabilize of I_C is success is measured by the stability factors. The stability factor is defined as the rate of change of collector current I_C with respect to the leakage current I_{co}, holding both β and V_{BE} constant.

8. **Define thermal runaway.**

The reverse saturation current I_{co} increases with increase in temperature. Specifically it double for every 10° rise in temperature. When I_{co} increase, the collector current I_C increase which increase the power dissipation. This increase in power dissipation increases the temperature, which further increase temperature. The process is cumulative and may results in permanent damage to the transistor. This is called thermal runaway.

9. **List the advantage and disadvantages of fixed bias method**

The advantages of fixed bias method are

(a) The stability of operating point is greatly improved when compared with other circuits.

(b) low cost and simple circuits.

The disadvantages of fixed bias methods are

(a) The stability is poor.

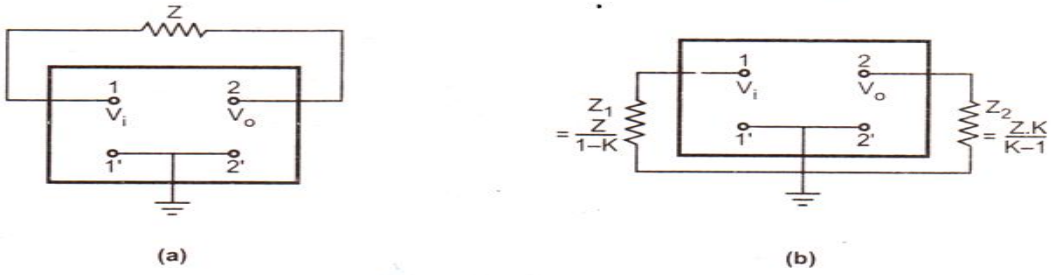
(b) When temperature changes, β changes and there by I_c and V_{CE} also increases which leads to thermal run away.

10. **Which is known as Universal bias?**

Voltage divider bias.

11.Write short notes on Miller's theorem.

In general, the Miller theorem is used for converting any circuit having configuration of Fig. 2.67 (a) to another configuration shown in Fig. 2.67 (b).



(a) (b)

Fig. 2.67 (a) and (b)

The Fig. 2.67 shows that, if Z is the impedance connected between two nodes, node 1 and node 2, it can be replaced by two separate impedances Z_1 and Z_2; where Z_1 is connected between node 1 and ground and Z_2 is connected between node 2 and ground.

The V_i and V_o are the voltages at the node 1 and node 2 respectively. The values of Z_1 and Z_2 can be derived from the ratio of V_o and V_i (V_o / V_i), denoted as K. Thus it is not necessary to know the values of V_i and V_o to calculate the values of Z_1 and Z_2.

The values of impedances Z_1 and Z_2 are given as

$$Z_1 = \frac{Z}{1-K} \quad \ldots (1)$$

and

$$Z_2 = \frac{Z \cdot K}{K-1} \quad \ldots (2)$$

FUNDAMENTALS OF ELECTRONIC ENGINEERING (FEE)

Subject Code: **L/T/P/C**
2/0/1/3
Int: 30, Ext: 70, Total: 100

Prerequisites:
- Fundamentals of Modern Physics
- Fundamentals of Electrical Networks

Course Objectives:
- To provide clear explanation of the working principles of important electronic devices
- To show how each device is used in appropriate circuits
- To demonstrate how such circuits are designed

Course Outcomes:
- Ability to get familiar knowledge on several Semiconductor Devices.
- Ability to analyze the working operation of each device in a circuit.
- Ability to compare the performance of devices in various applications.

UNIT-I

Semiconductors and pn Junction Diode: Semi conductor Physics: n and p type semi conductors, Mass Action Law, Continuity Equation, Hall Effect, Fermi level in intrinsic and extrinsic semiconductors, Open- circuited p-n junction, Energy band diagram of PN diode, forward bias and reverse bias, Current components in p-n diode, Law of junction, Diode equation, Volt-ampere characteristics of p-n diode, Temperature dependence of V-I characteristic, Transition and Diffusion capacitances, Breakdown Mechanisms in Semi Conductor Diodes (Avalanche and Zener breakdown), Zener diode characteristics,

UNIT-II

Diode Applications, Special Diodes: Half wave rectifier, ripple factor, full wave rectifier, Harmonic components in a rectifier circuit, Inductor filter, Capacitor filter, L- section filter, Π- section filter, and comparison of various filter circuits in terms of ripple factors, Simple circuit of a regulator using zener diode, Series and Shunt voltage regulators

Special Diodes: Characteristics of Tunnel Diode, Varactor Diode, LED, LCD.

UNIT-III

Bipolar Junction Transistor: Junction transistor, Transistor current components, Transistor as an amplifier, Transistor construction, Detailed study of currents in a transistor, Input and Output characteristics of transistor in Common Base, Common Emitter, and Common collector configurations, Relation between Alpha and Beta and Gamma, typical transistor junction voltage values,

Junction Field Effect Transistors (JFET): JFET characteristics (n and p channels), Small signal model of JFET, MOSFET characteristics (Enhancement and depletion mode), Introduction to SCR and UJT.

UNIT-IV

Biasing and stabilization : BJT biasing, DC equivalent model, criteria for fixing operating point, Fixed bias, Collector to base bias, Self bias techniques for stabilization, Stabilization factors, Compensation techniques, Compensation against variation in V_{BE} and I_{CO}, Thermal run away, Thermal stability.

UNIT-V

Amplifiers: Small signal low frequency transistor amplifier circuits: h-parameter representation of a transistor, Analysis of single stage transistor amplifier using h-parameters: voltage gain, current gain, Input impedance and Output impedance. Comparison of transistor configurations in terms of Ai, Ri, Av, Ro.

Teaching methodologies:
- Power Point presentations
- Tutorial Sheets
- Assignments
- Lab experiments with Multisim software

Text Books:
1. David A. Bell; Electronic Devices and Circuits, Oxford University Press, 5th edition, 2008.
2. R.L. Boylestad and Louis Nashelsky; Electronic Devices and Circuits, Pearson/Prentice Hall, 9th Edition, 2006.

References:
1. T.F. Bogart Jr J.S.Beasley and G.Rico; Electronic Devices and Circuits – Pearson Education, 6th edition, 2004.